

**1200-Output Channel  
TFT LCD Source Driver with TCON**

**Specification**  
*Preliminary*

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**ILI TECHNOLOGY CORP.**

8F., No.1, Taiyuan 2nd St., Zhubei City,  
Hsinchu County 302, Taiwan (R.O.C.)  
Tel.886-3-5600099; Fax.886-3-5670585  
<http://www.ilitek.com>

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## 1. Introduction

ILI6137A is a 1200-channel output source driver with TTL interface timing controller (TCON). The interface follows digital 24-bit parallel RGB input format. The TCON generates the 800x480 and 800x600 resolutions and provides horizontal and vertical control timing to source driver and gate driver. It also supports dithering feature, apply source driver with 6-bit DAC to perform 8-bit resolution 256 gray scales. Operating parameters can be set via pin control for all control features. Since the output circuit of this source driver incorporates an operational amplifier with low power dissipation, and performs wide voltage supply range and small output deviation.

ILI6137A can be configured as dual-gate operation mode for reducing FPC amount and saving the cost. With wide range of supply voltages and many pin control features make this chip mode suitable for various applications.

## 2. Features

### ◆ TCON

- Supports display resolution 800x480 and 800x600
- Supports digital 24-bit parallel RGB input mode
- Source output with 8-bit resolution for 256 gray scales (2-bit dithering)
- Supports dual-gate operation mode
- Supports Stripe CF configuration
- Maximum Operation frequency: 50 MHz
- Provide flip and mirror scan mode by pin control
- Supports stand-by mode for saving power consumption
- Operation Voltage Level 3.0V to 3.6V

### ◆ Source Driver

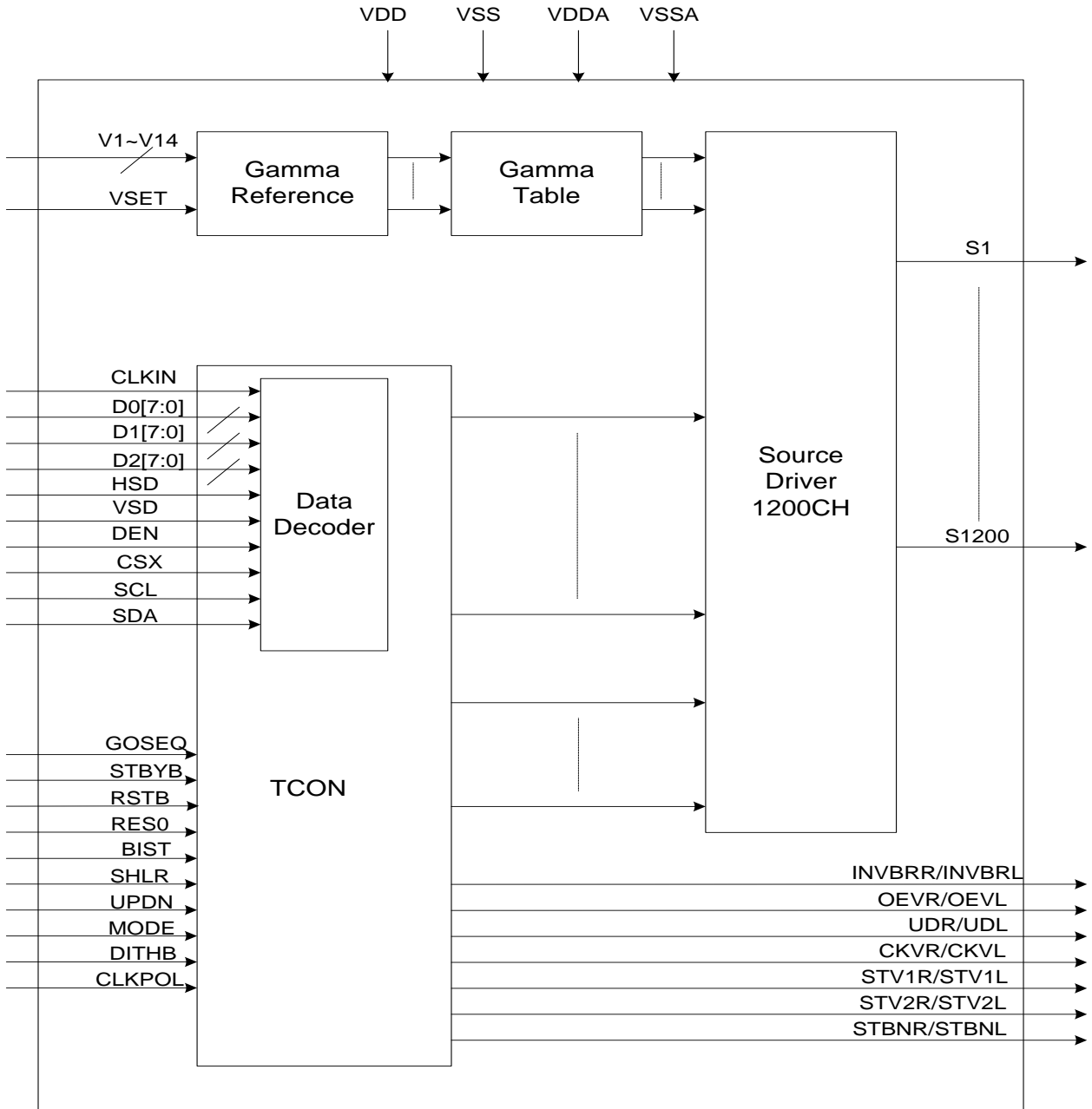
- 1200 channels output source driver for TFT LCD panel
- Embedded custom-made Gamma table for special custom request
- Supports external V1~V14 pad for Gamma adjustment
- Output dynamic range : 0.1 ~ VDDA-0.1V
- Voltage deviation of outputs:  $\pm 20\text{mV}$
- Power for source driver voltage (VDDA) : 8.5V ~ 13.5V

### ◆ Others

- COG package

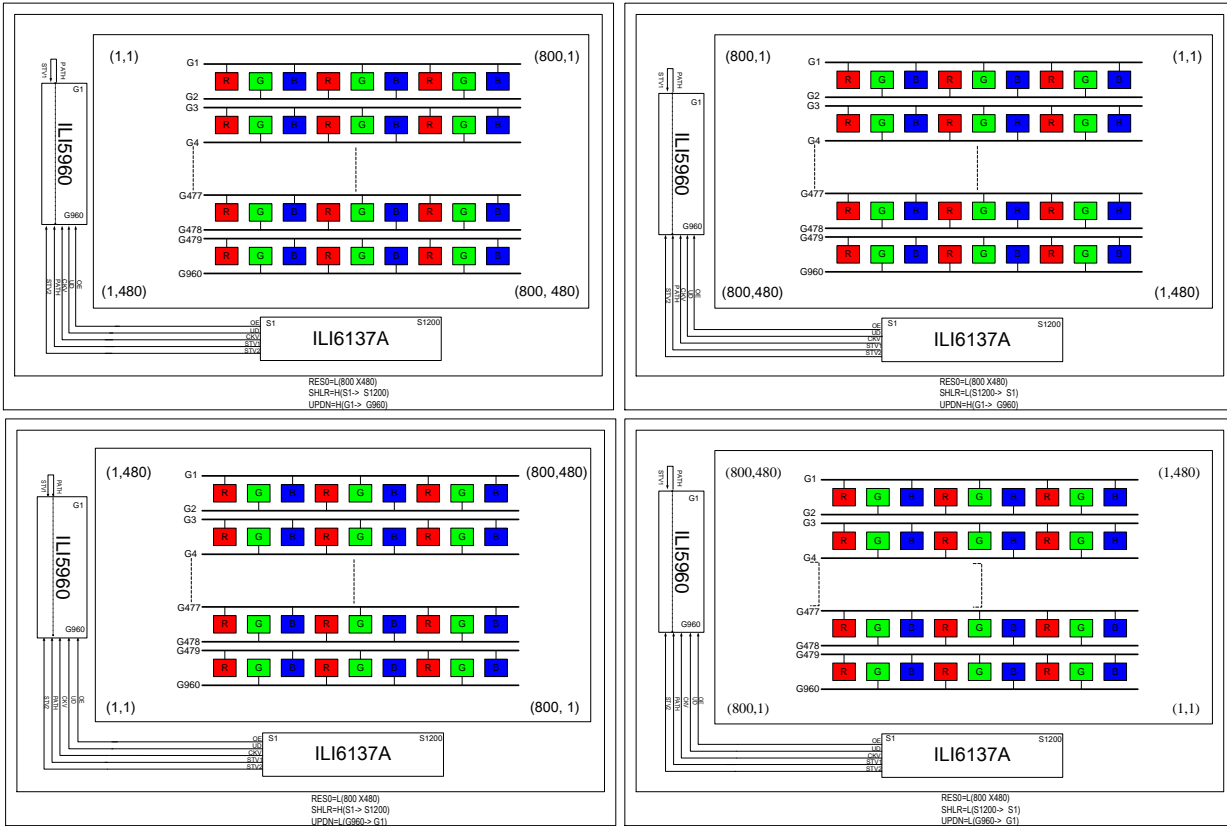
### 3. Block Diagram

#### 3.1. Function Block Diagram

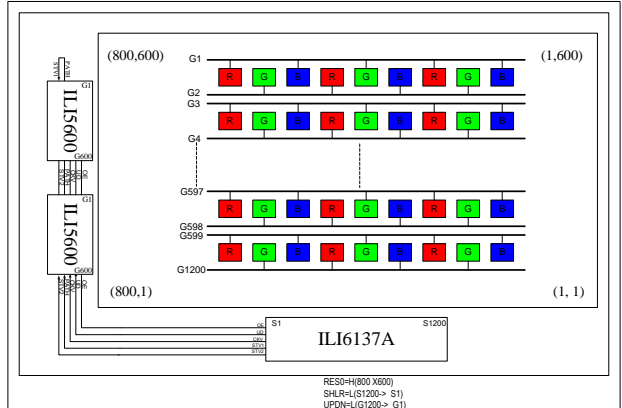
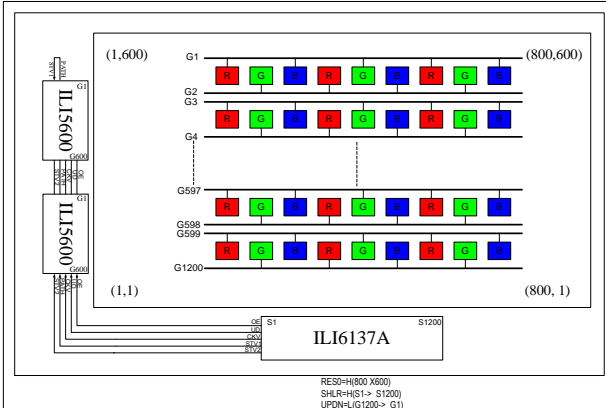
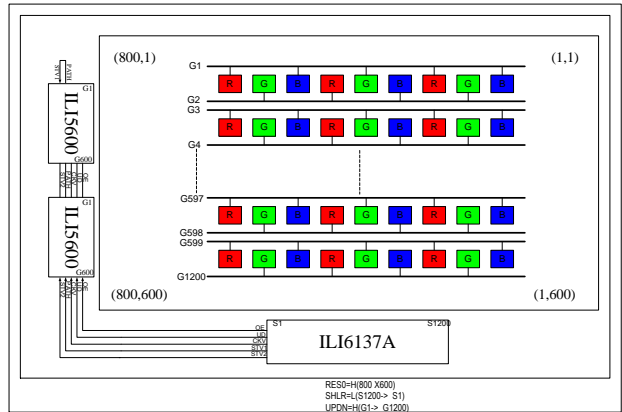
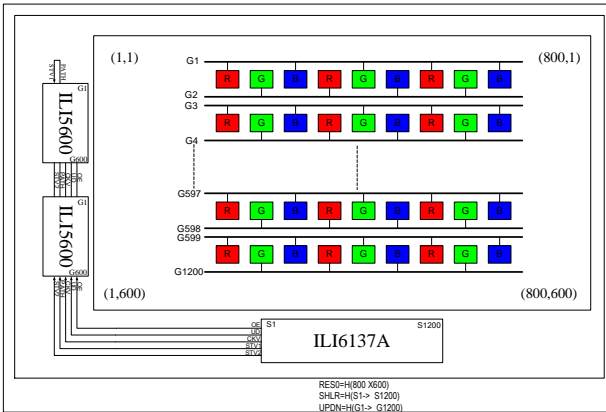


### 3.2. Application Block Diagram

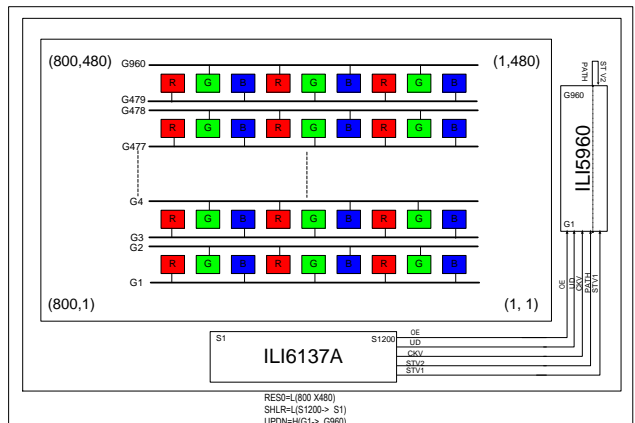
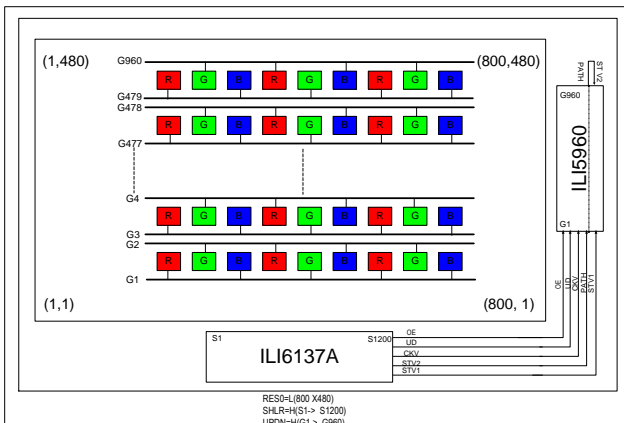
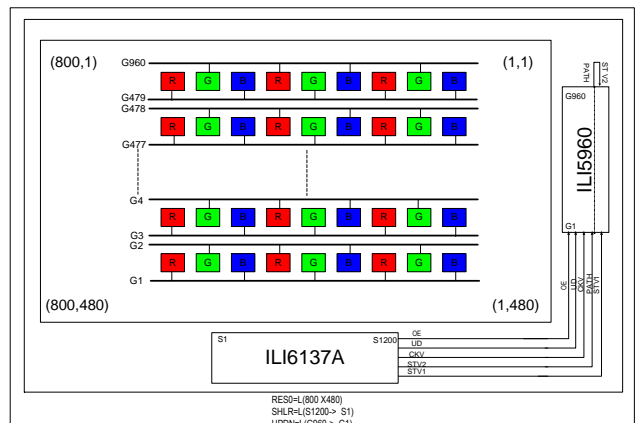
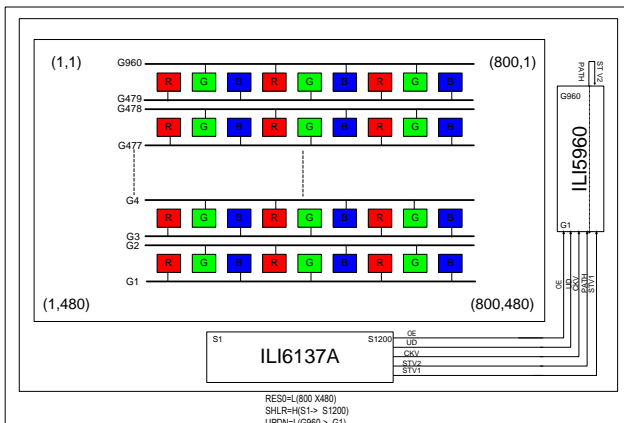
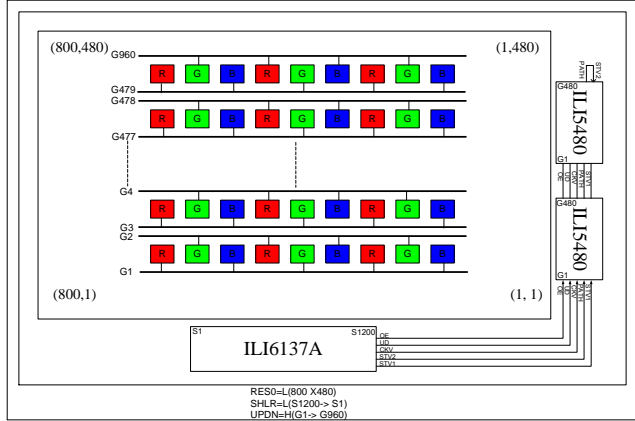
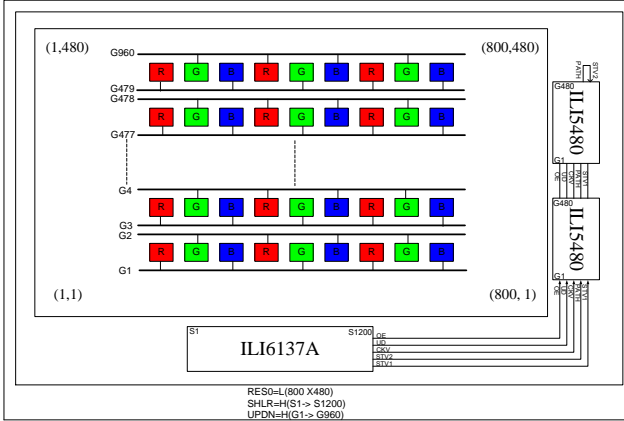
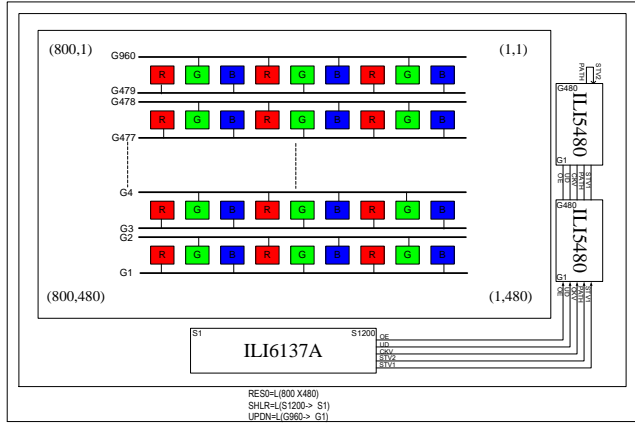
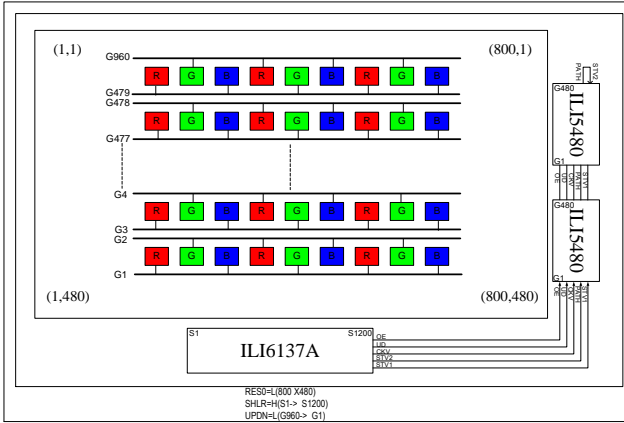
#### 3.2.1. 800(RGB) x 480 (Gate driver on left side)



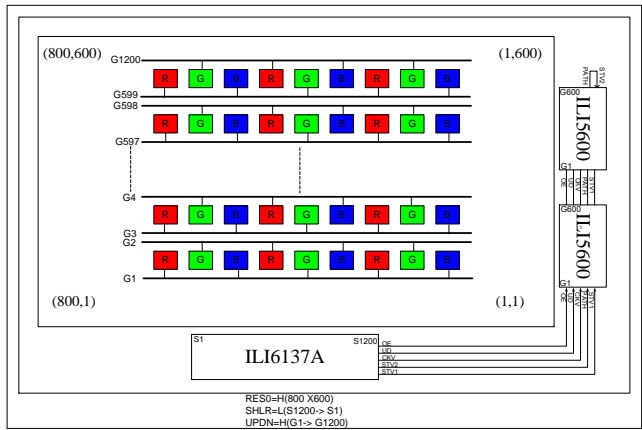
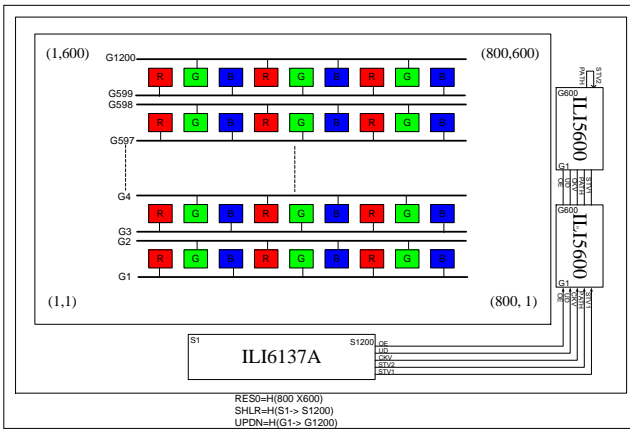
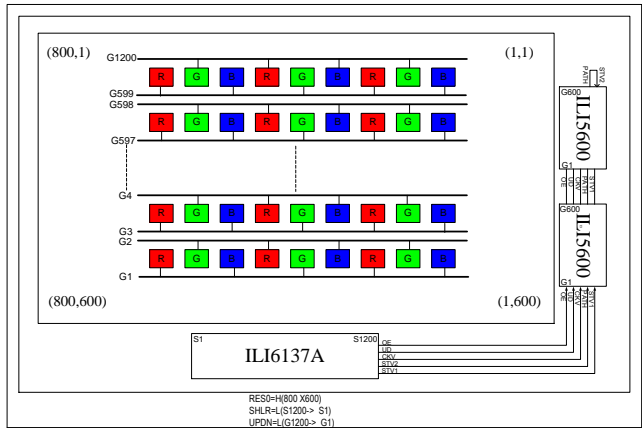
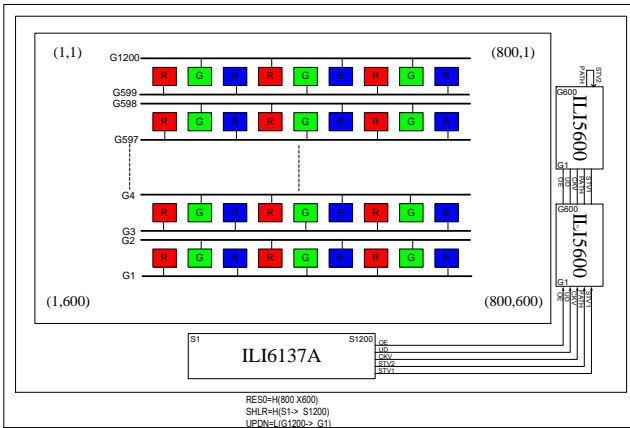
**3.2.2. 800(RGB) x 600 (Gate driver on left side)**



**3.2.3. 800(RGB) x 480 (Gate driver on right side)**



**3.2.4. 800(RGB) x 600 (Gate driver on right side)**





## 4. Pin Descriptions

Pin Name	I/O	Descriptions
CLKIN	I	Clock for input data. Data latched at rising/falling edge of this signal. Default is falling edge.
D0[7:0] D1[7:0] D2[7:0]	I	Digital data input. Dx0 is LSB and Dx7 is MSB. D0[7:0] = R[7:0] data; D1[7:0] = G[7:0] data; D2[7:0]=B[7:0] data. When 18-bit RGB interface (disable dithering function), please use Dx[7:2] as 6-bit input and connect Dx[1:0] to VSS.
HSD	I	Horizontal sync input in digital parallel RGB. Negative polarity.
VSD	I	Vertical sync input in digital parallel RGB. Negative polarity.
DEN	I	Input data enable control. When DE mode, active High to enable data input. (Normally pull low)
MODE	I	DE / SYNC mode select. (Normally pull high) MODE="L", for entering SYNC mode. MODE="H", for entering DE mode.
CSX	I	Reserved pins, not accessible to user. (Normally pull high)
SCL	I	Reserved pins, not accessible to user. (Normally pull high)
SDA	I/O	Reserved pins, not accessible to user. (Normally pull high)
RSTB	I	Hardware global reset. Low active. (Normally pull high)
RES0	I	Display resolution selection. (Normally pull low) RES0="L", for 800(RGB)x480 display resolution. RES0="H", for 800(RGB)x600 display resolution.
DITHB	I	Dithering function enable control. (Normally pull high) DITHB="L", to enable internal dithering function. DITHB="H", to disable internal dithering function.
CLKPOL	I	Input clock edge selection. (Normally pull low) CLKPOL="L", latch data at CLKIN falling edge. CLKPOL="H", latch data at CLKIN rising edge.
V1 ~ V14	I/O	When VSET="L", the internal Gamma table is used and V1~V14 pins are unused. When VSET="H", V1~V14 pins are the external adjustment point for Gamma correction. The relationship between V1~V14 must be : VSSA<V14<V13<V12<V11<V10<V9<V8<V7<V6<V5<V4<V3<V2<V1<VDDA
GOSEQ	I	Gate on sequence. (Normally pull low) GOSEQ="L", INVBRR/INVBRL will output "H" and gate on sequence is "G1→G2→G3→G4→G5→G6→G7→G8→.....→G <sub>n-3</sub> →G <sub>n-2</sub> →G <sub>n-1</sub> →G <sub>n</sub> "

Pin Name	I/O	Descriptions
		GOSEQ="H", INVBRR/INVBRL will output "L" and gate on sequence is "G1→G2→G4→G3→G5→G6→G8→G7→.....→G <sub>n-3</sub> →G <sub>n-2</sub> →G <sub>n</sub> →G <sub>n-1</sub> "
VSET	I	Gamma correction source select. (Normally pull low) VSET="L", to use internal Gamma reference voltage (VDDA). VSET="H", to use external Gamma correction input (V1~V14).
STBYB	I	Standby mode control. (Normally pull high) STBYB="L", enter standby mode for power saving. Timing controller and source driver will turn off, all outputs are Hi-Z. STBYB="H", normal operation.
SHLR	I	Source shift direction control. (Normally pull high) SHLR="L", shift direction is "S1200 → S1199 → 1198 → ... S3 → S2 → S1" SHLR="H", shift direction is "S1 → S2 → S3 → ... → S1198 → S1199 → S1200".
UPDN	I	Gate scan direction control (Normally pull low) UPDN="L", STV2 outputs the vertical start pulse and UD pin outputs "L" to Gate driver. UPDN="H", STV1 outputs the vertical start pulse and UD pin outputs "H" to Gate driver.
BIST	I	Normal operation / BIST pattern select. (Normally pull low) BIST="L", Normal operation BIST="H", BIST (DCLK input is not needed)
BLKEN	O	The backlight control signal for external backlight controller. BLKEN="L", turn off the external backlight controller. BLKEN="H", turn on the external backlight controller.
OEVR OEVL	O	Gate driver control signal.
UDR UDL	O	Gate driver control signal.
CKVR CKVL	O	Gate driver control signal.
STV1R STV1L	O	Gate driver control signal.
STV2R STV2L	O	Gate driver control signal.
STBNR STBNL	O	Gate driver control signal.
INVBRR INVBRL	O	Gate driver control signal.

Pin Name	I/O	Descriptions
VDDA	P	Power supply for analog block.
VSSA	P	Ground level for analog block.
VDD	P	Power supply for digital block.
VSS	P	Ground level for digital block.
S1 ~ S1200	O	Source driver output signals.
ALIGN	--	For assembly alignment.
COM1_B COM2_B	--	COM1_B and COM2_B are short-circuited within ILI6137A for contact resistance measurement. Please leave it open when not in use.
COM1_T COM2_T	--	COM1_T and COM2_T are short-circuited within ILI6137A for contact resistance measurement. Please leave it open when not in use.
TP0 ~ TP4	I	Test pins, not accessible to user.
TP5	I	TP5 pin: Normal black/Normal white data reversed pin. HIGH- Normal black , LOW- Normal white
TP6 ~ TP10	O	Test pins, not accessible to user.
SHIELDING	--	IC shielding pads. Those pins are internally connected to VSSA level.
TN0, TN1, TN8, TN9	-	Reserved pins, not accessible to user.
TN2 ~ TN5, TN7	I	Reserved pins, not accessible to user.
DASHD	--	Data bus shielding pad. Those pins are internally connected to VSS level.
DUMMY	--	Dummy pads. Please leave it open when not in use.

Note: (1) Please power on following the sequence VDD → logic input → VDDA and V1 ~ V14. Reverse the sequence to shut down.

(2) To stabilize the supply voltages, please be sure to insert a 0.1uF bypass capacitor between VDD↔VSS and VDDA↔VSSA. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01uF is also advised between the gamma-corrected power supply terminals (V1, V2, ..., V14) and VSSA.

(3) Please keep V1~V14 not cross to the toggle signals as possible to avoid the AC coupling on the DC V1~V14 voltage. When used as cascade mode, please keep the coupled amount of V1~V10 are the same between the two chips.

(4) The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommended as below.

Pin Name	Wiring resistance value( $\Omega$ )
VDDA	< 5
VSSA	< 5
VDD	< 10
VSS	< 10
V1 ~ V14	< 10
Dx[0:7]	< 50
CLKIN	< 50
VSD	< 50
HSD	< 50
DEN	< 50
BLKEN	< 200
CSX	< 200
SCL	< 200
SDA	< 200
RSTB	< 500
STBYB	< 500
DITHB	< 500
SHLR	< 500
UPDN	< 500
BIST	< 500
MODE	< 500
RES0	< 500
CLKPOL	< 500
VSET	< 500
INVBRR / INVBRL	< 500
OEVR / OEVL	< 500
UDR / UDL	< 500
CKVR / CKVL	< 500
STV1R / STV1L	< 500
STV2R / STV2L	< 500
STV2R / STV2L	< 500
STBNR / STBNL	< 500
Others	< 500

## 5. Operation Description

### 5.1. Relationship between input data and output channels

#### 5.1.1. Stripe Mode

The relationship between input display data and source output channels is illustrated as below:

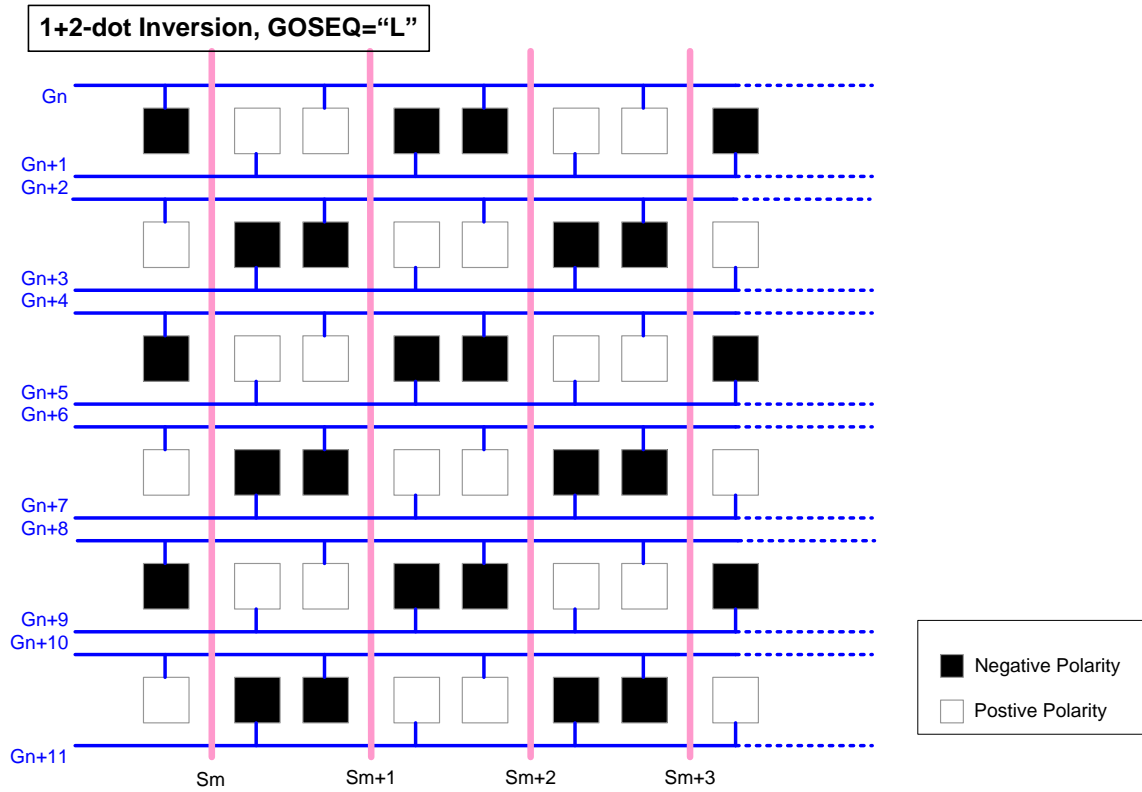
SHLR="L", Left Shift Direction							
Output	S1	S2	S3	←	S1198	S1199	S1200
Order	Last data			---	First data		
Odd Line / $G_n$	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Odd Line / $G_{n+1}$	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]
Even Line / $G_n$	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Even Line / $G_{n+1}$	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]

SHLR="H", Right Shift Direction							
Output	S1	S2	S3	→	S1198	S1199	S1200
Order	First data			---	Last data		
Odd Line / $G_n$	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Odd Line / $G_{n+1}$	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]
Even Line / $G_n$	D0[7:0]	D2[7:0]	D1[7:0]	---	D0[7:0]	D2[7:0]	D1[7:0]
Even Line / $G_{n+1}$	D1[7:0]	D0[7:0]	D2[7:0]	---	D1[7:0]	D0[7:0]	D2[7:0]

### 5.2. Dot Polarity Inversion

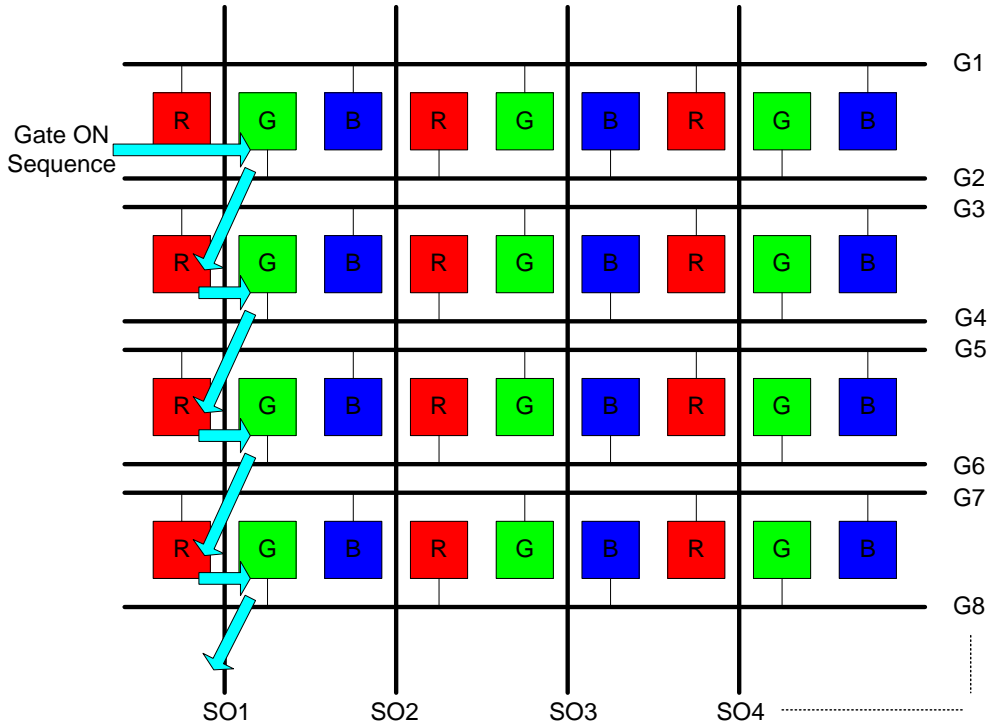
ILI6137A supplies 1+2-dot inversion, the pixel polarity inversion was illustrated as below:



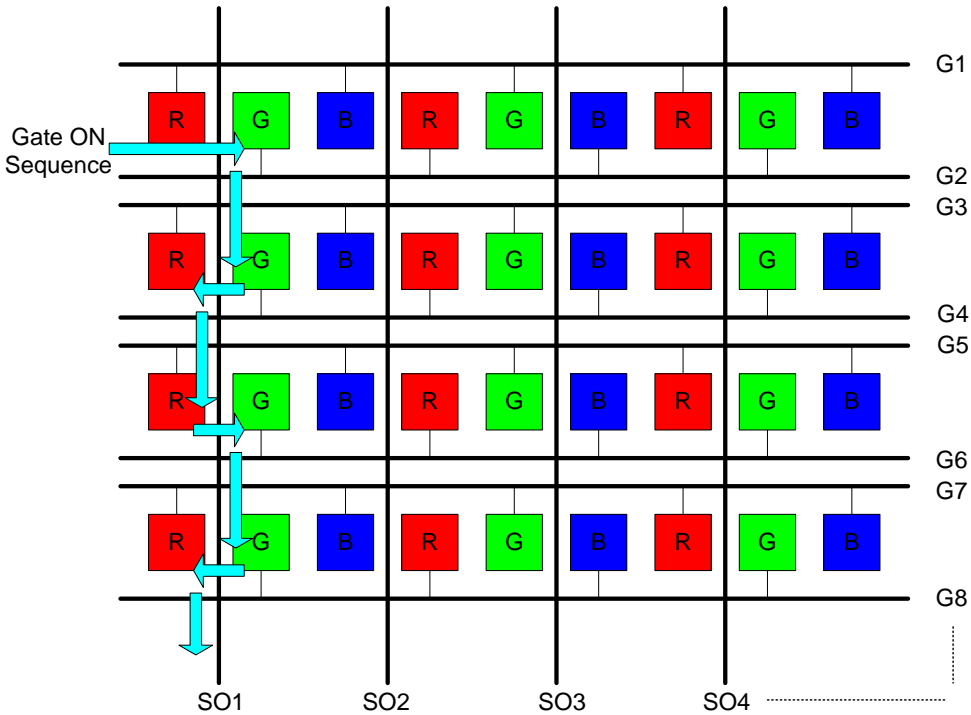
**5.3. Gate Scan Sequence**

Based on special panel request, ILI6137A supports two kinds of gate scan sequences and illustrated as below:

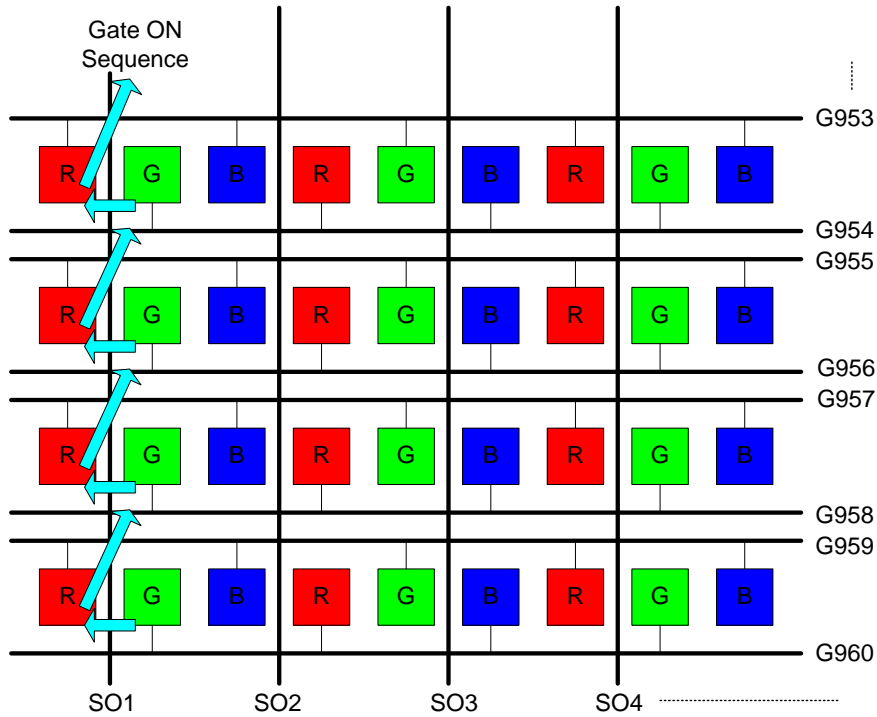
**GOSEQ="L", UPDN="H" → INVBR/INVBRL="H" (Traditional Scan, For General Gate Driver)**



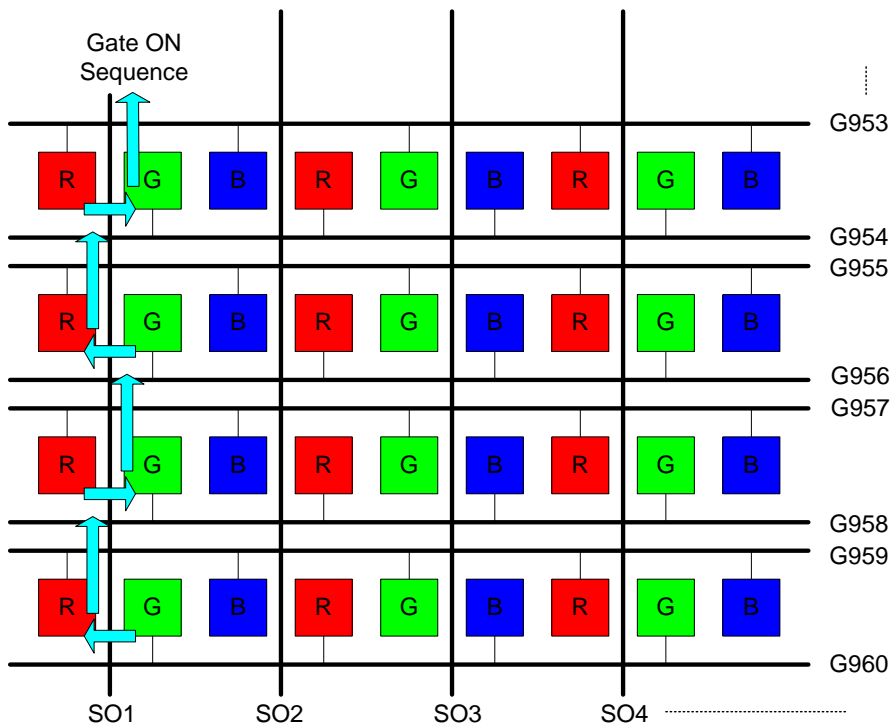
**GOSEQ="H", UPDN="H" → INVBR/INVBRL="L" (Bow-shaped Scan, For Special Gate Driver)**



**GOSEQ="L", UPDN="L" → INVBRR/INVBRL="H" (Traditional Scan, For General Gate Driver)**



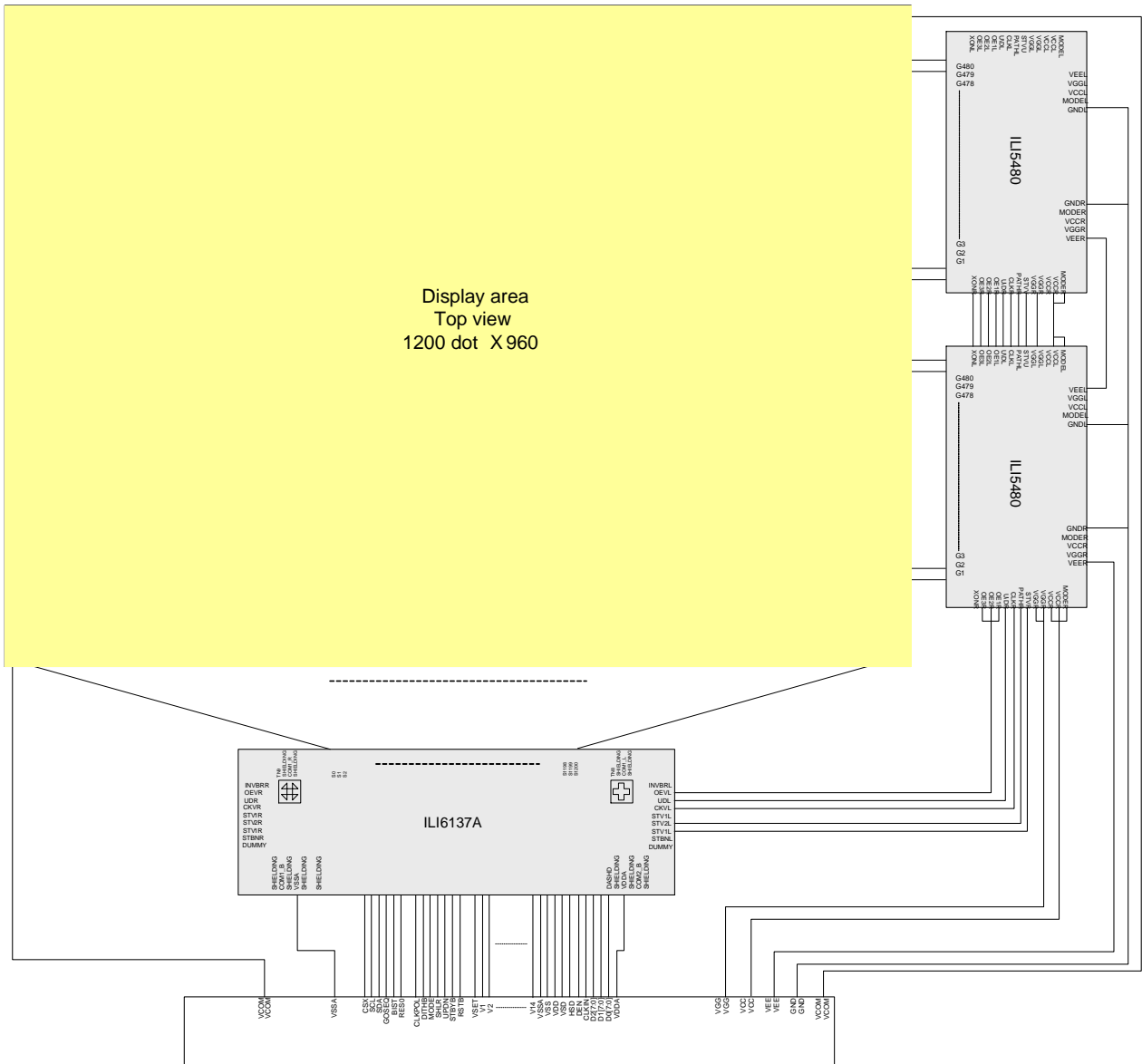
**GOSEQ="H", UPDN="L" → INVBRR/INVBRL="L" (Bow-shaped Scan, For Special Gate Driver)**





### 5.4. Application Block Diagram

The configuration examples 800(RGB)\*480 of the ILI6137A are illustrated as the following figure.



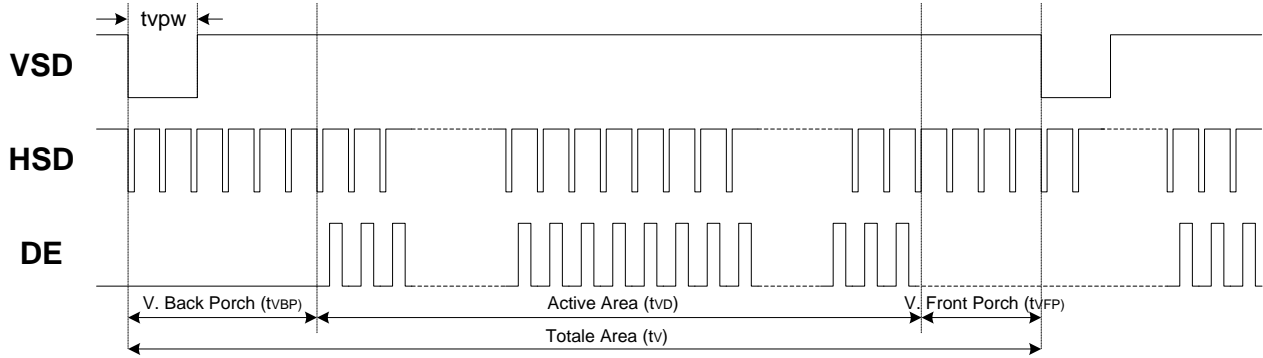




## 5.5. Display Data Input Timing

### 5.5.1. Vertical Input Timing

ILI6137A provides two different interface modes, SYNC mode and DE mode. Both modes can be selected by MODE pin, ILI6137A will enter the SYNC mode while MODE pin is set to 'L' and enter DE mode while MODE pin is set to 'H'.



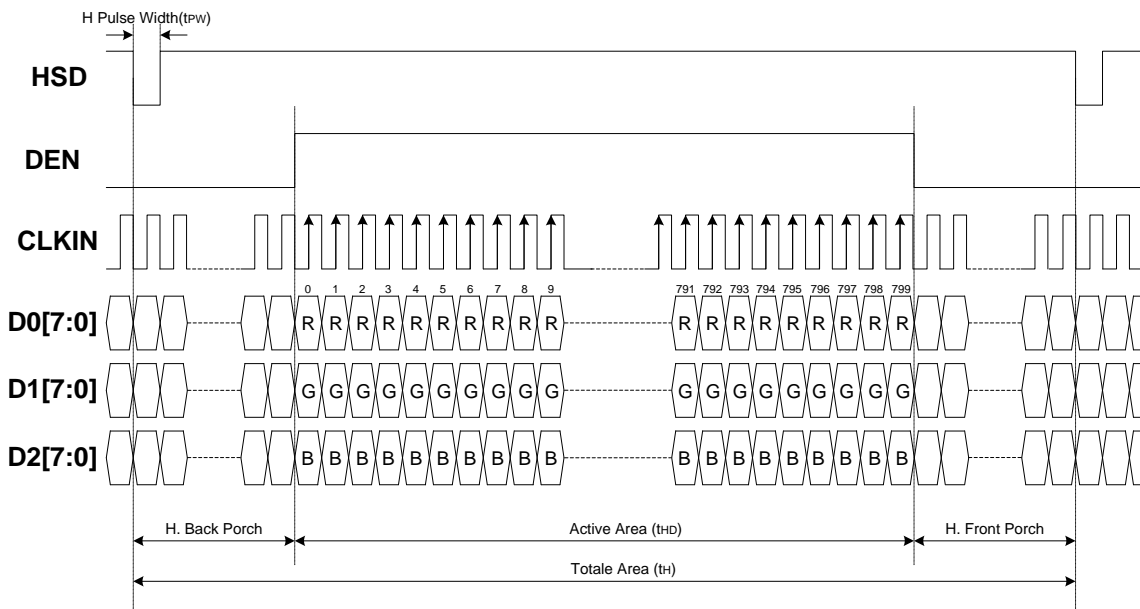
### 5.5.2. Horizontal Input Timing

#### 5.5.2.1. SYNC Mode (MODE="L")

ILI6137A will enter SYNC mode while MODE pin is fixed at "L" level. Every HSD period is consists of Horizontal Back Porch, Active Area and Horizontal Front Porch time. The first active display data is transmitted at the first falling/rising edge of CLKIN after Horizontal Back Porch period and the last display data is transmitted at the last falling/rising edge of CLKIN before Horizontal Front Porch period.

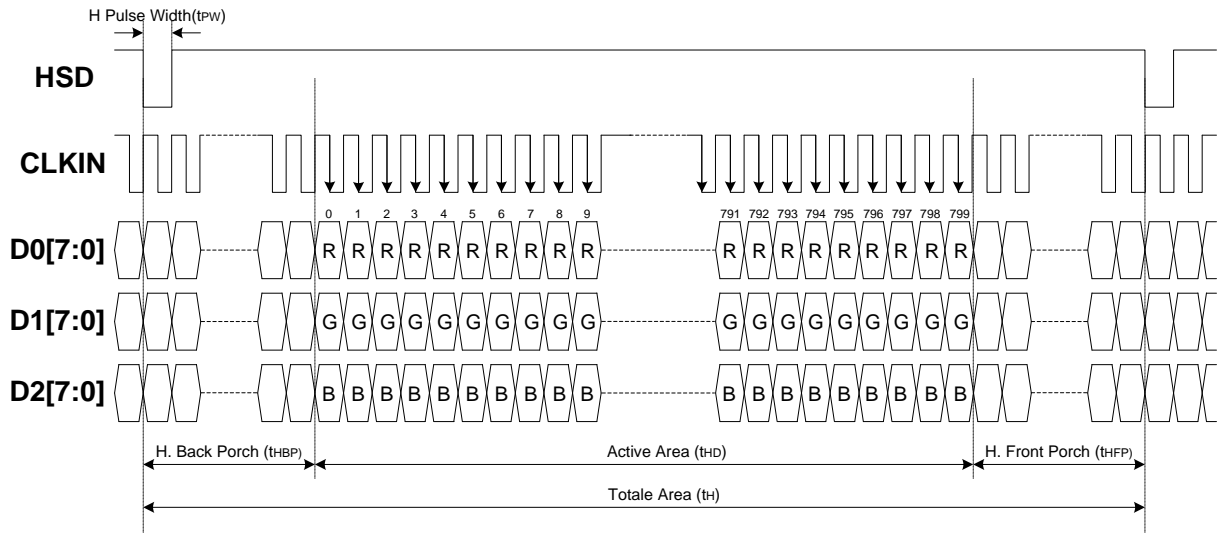
#### 5.5.2.2. DE Mode (MODE="H")

ILI6137A will enter DE mode while MODE pin is fixed at "H" level. ILI6137A will treat the data on Dx[7:0] bus as active display data while DEN is at "H" level and ignore the data on Dx[7:0] bus while DEN is at "L" level.



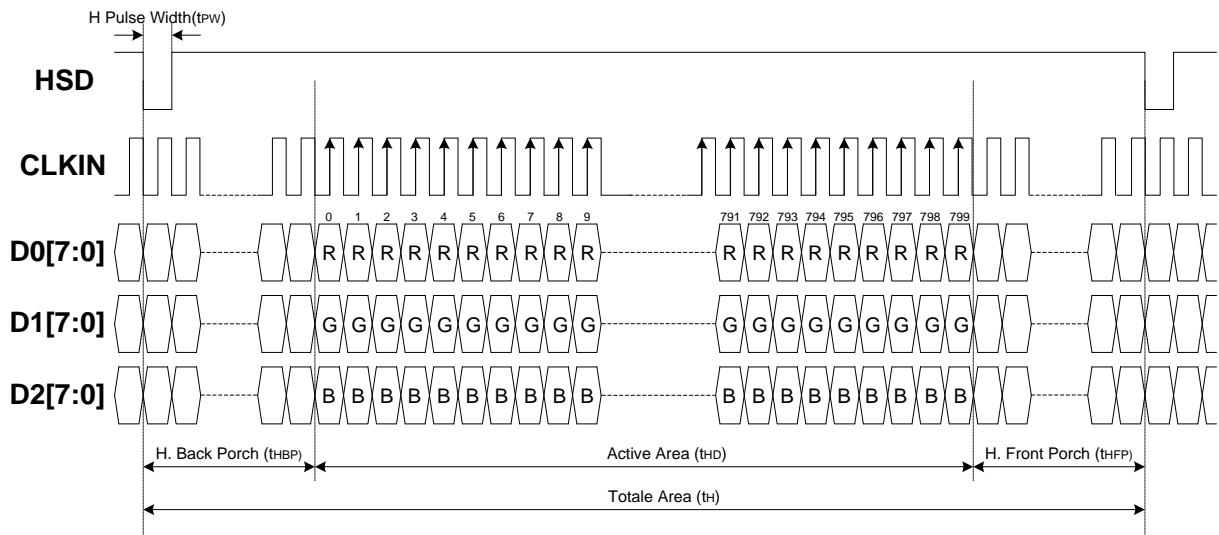
ILI6137A will latch the display data on Dx[7:0] bus at falling edge of CLKIN when CLKPOL is set to “L”, the input data timing is illustrated as below:

**CLKPOL= “L”**



ILI6137A will latch the display data on Dx[7:0] bus at rising edge of CLKIN when CLKPOL is set to “H”, the input data timing is illustrated as below:

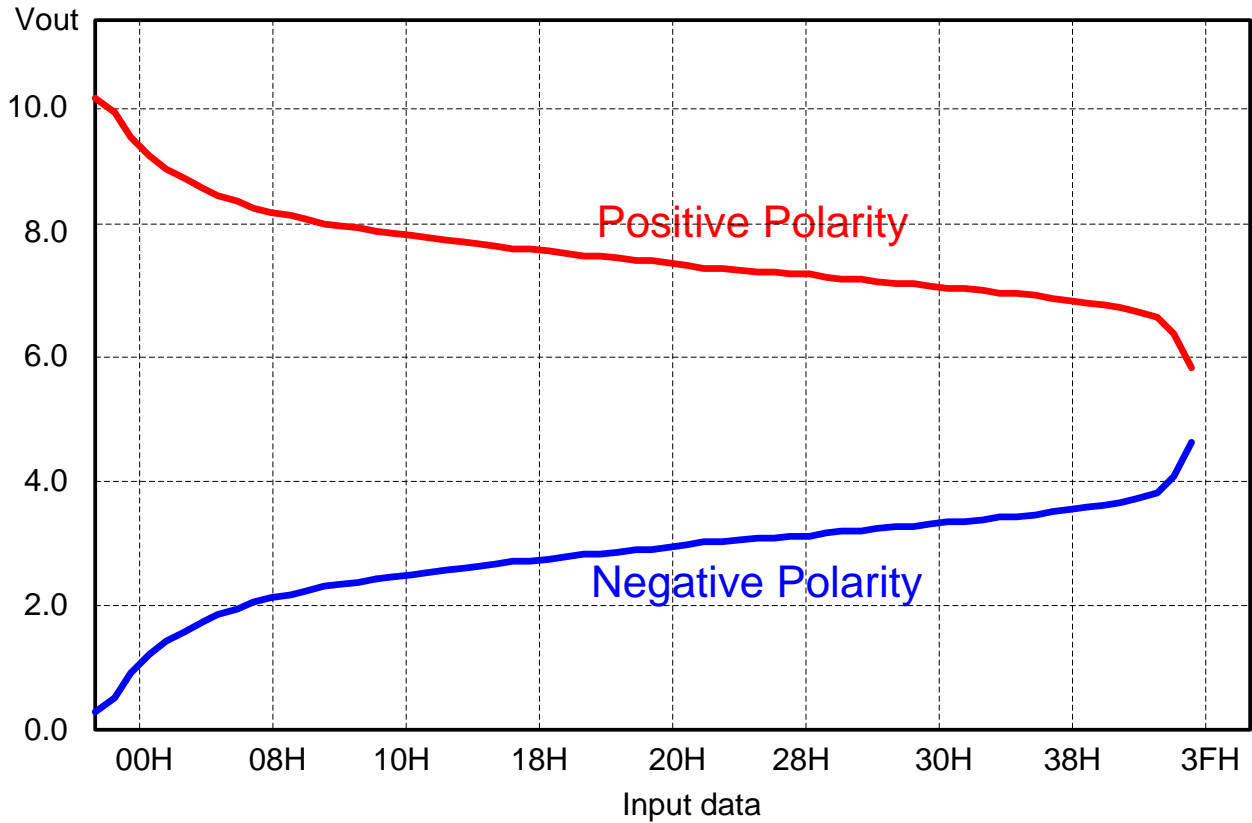
**CLKPOL= “H”**



**5.6. Relationship between gamma correction and output voltage**

The output voltage is determined by the 6-bit digital input data, and the V1 ~ V14 gamma correction reference voltage inputs. The figure in the following shows the relationship between the input data and the output voltage. Refer the next page for the relative values and voltage calculation method.

Gamma correction characteristic curve:



Note :  $V_{DDA}-0.1 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V6 \geq V7 \geq V8 \geq V9 \geq V10 \geq V11 \geq V12 \geq V13 \geq V14 \geq V_{SSA}+0.1$

The internal Gamma Table is shown as below. (VSET="L")

Display Data (Hex)	Positive Polarity	Negative Polarity
00h	VDDA x 0.961	VDDA x 0.019
01h	VDDA x 0.937	VDDA x 0.045
02h	VDDA x 0.903	VDDA x 0.081
03h	VDDA x 0.880	VDDA x 0.106
04h	VDDA x 0.861	VDDA x 0.126
05h	VDDA x 0.847	VDDA x 0.142
06h	VDDA x 0.836	VDDA x 0.155
07h	VDDA x 0.826	VDDA x 0.166
08h	VDDA x 0.818	VDDA x 0.176
09h	VDDA x 0.810	VDDA x 0.184
0Ah	VDDA x 0.804	VDDA x 0.192
0Bh	VDDA x 0.798	VDDA x 0.199
0Ch	VDDA x 0.793	VDDA x 0.205
0Dh	VDDA x 0.788	VDDA x 0.211
0Eh	VDDA x 0.783	VDDA x 0.217
0Fh	VDDA x 0.779	VDDA x 0.222
10h	VDDA x 0.775	VDDA x 0.227
11h	VDDA x 0.772	VDDA x 0.231
12h	VDDA x 0.768	VDDA x 0.236
13h	VDDA x 0.765	VDDA x 0.240
14h	VDDA x 0.762	VDDA x 0.244
15h	VDDA x 0.759	VDDA x 0.248
16h	VDDA x 0.757	VDDA x 0.252
17h	VDDA x 0.754	VDDA x 0.256
18h	VDDA x 0.751	VDDA x 0.259
19h	VDDA x 0.749	VDDA x 0.263
1Ah	VDDA x 0.746	VDDA x 0.266
1Bh	VDDA x 0.744	VDDA x 0.269
1Ch	VDDA x 0.742	VDDA x 0.272
1Dh	VDDA x 0.740	VDDA x 0.276
1Eh	VDDA x 0.737	VDDA x 0.279
1Fh	VDDA x 0.735	VDDA x 0.282
20h	VDDA x 0.733	VDDA x 0.285
21h	VDDA x 0.731	VDDA x 0.288
22h	VDDA x 0.729	VDDA x 0.291
23h	VDDA x 0.728	VDDA x 0.294
24h	VDDA x 0.726	VDDA x 0.297
25h	VDDA x 0.724	VDDA x 0.300
26h	VDDA x 0.721	VDDA x 0.302
27h	VDDA x 0.719	VDDA x 0.305
28h	VDDA x 0.717	VDDA x 0.308
29h	VDDA x 0.716	VDDA x 0.311
2Ah	VDDA x 0.714	VDDA x 0.315
2Bh	VDDA x 0.713	VDDA x 0.318
2Ch	VDDA x 0.712	VDDA x 0.321
2Dh	VDDA x 0.710	VDDA x 0.325
2Eh	VDDA x 0.708	VDDA x 0.328
2Fh	VDDA x 0.707	VDDA x 0.331
30h	VDDA x 0.704	VDDA x 0.334
31h	VDDA x 0.702	VDDA x 0.337
32h	VDDA x 0.700	VDDA x 0.340
33h	VDDA x 0.698	VDDA x 0.344
34h	VDDA x 0.697	VDDA x 0.349
35h	VDDA x 0.695	VDDA x 0.353
36h	VDDA x 0.693	VDDA x 0.358
37h	VDDA x 0.692	VDDA x 0.363
38h	VDDA x 0.690	VDDA x 0.368
39h	VDDA x 0.688	VDDA x 0.374
3Ah	VDDA x 0.686	VDDA x 0.381
3Bh	VDDA x 0.683	VDDA x 0.389
3Ch	VDDA x 0.680	VDDA x 0.398
3Dh	VDDA x 0.675	VDDA x 0.408
3Eh	VDDA x 0.664	VDDA x 0.423
3Fh	VDDA x 0.604	VDDA x 0.489

VDDA=10.4V		
V <sub>GMA</sub>	Code	Voltage
V1	00h	9.99 V
V2	01h	9.74 V
V3	10h	8.06 V
V4	20h	7.62 V
V5	30h	7.32 V
V6	3Eh	6.91 V
V7	3Fh	6.28 V
V8	3Fh	5.09 V
V9	3Eh	4.40 V
V10	30h	3.47 V
V11	20h	2.96 V
V12	10h	2.36 V
V13	01h	0.47 V
V14	00h	0.198 V

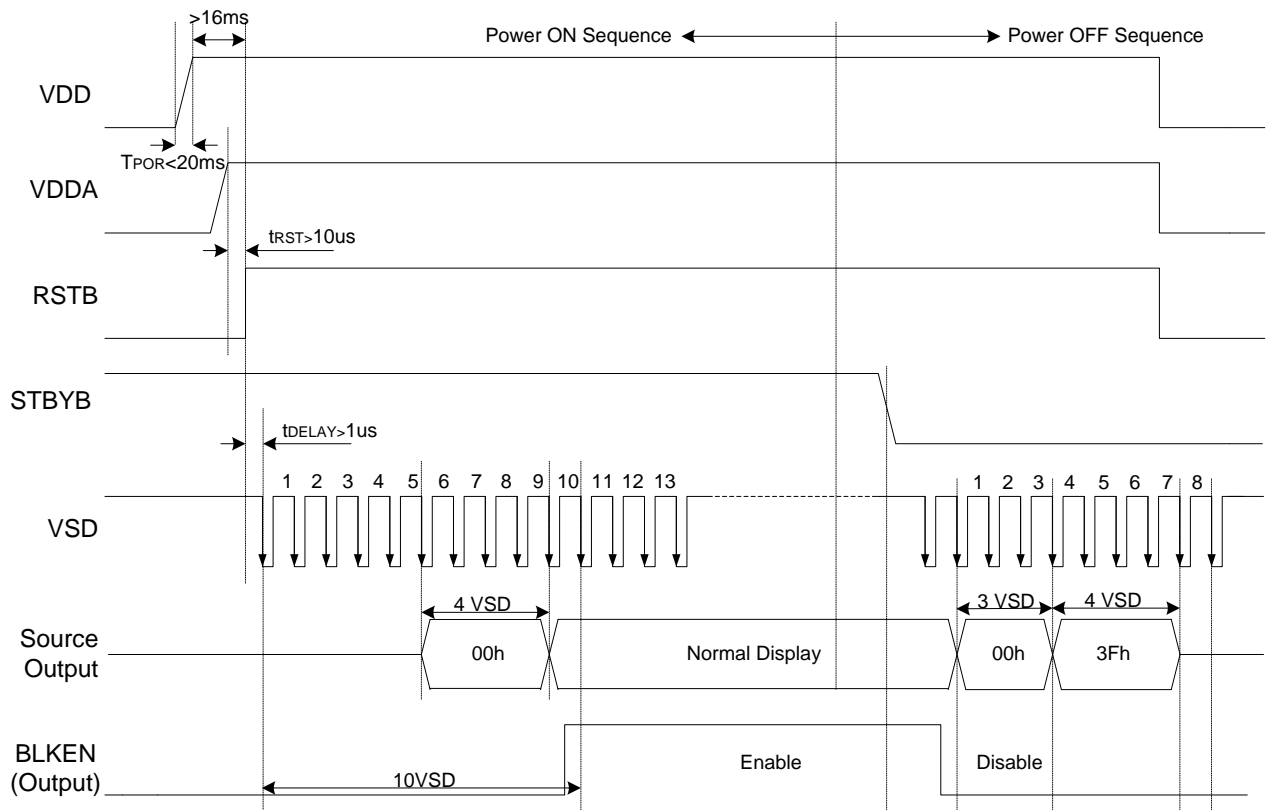
### 5.7. Power ON/OFF Sequence

To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.

Power ON: VDD, VSS → VDDA, VSSA → V1 to V14

Power OFF: V1 to V14 → VDDA, VSSA → VDD, VSS

In order to prevent ILI6137A from power ON reset fail, the rising time ( $t_{POR}$ ) of the digital power supply VDD should be maintained within given specifications. The power ON/OFF timing sequence is illustrated as below:

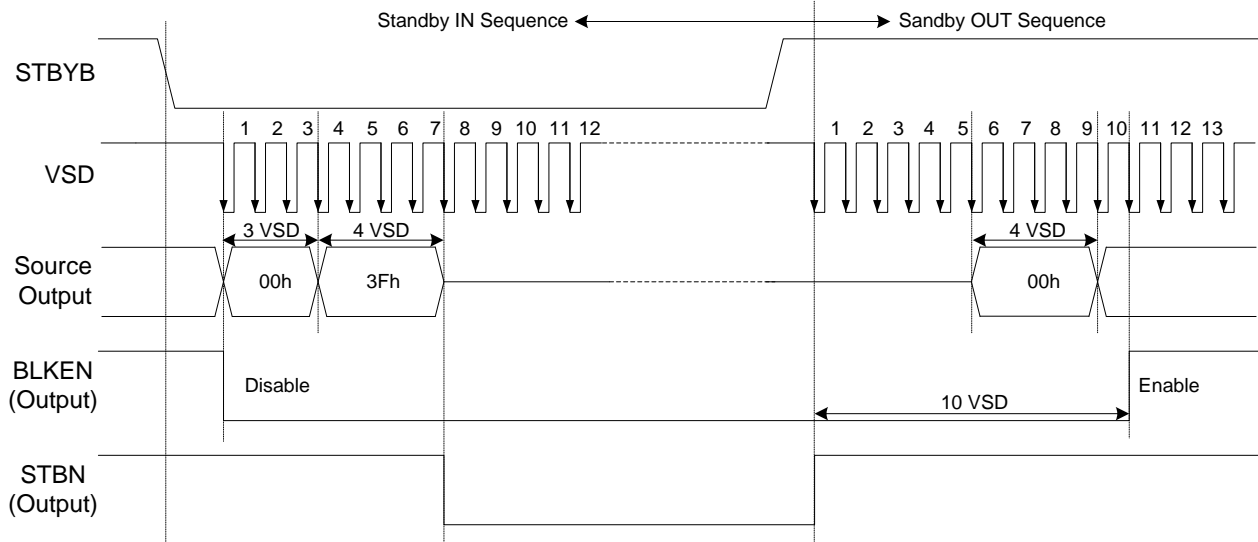


Note: For preventing abnormal operation,  $t_{RST}$  must be longer than 10us during Power ON sequence.




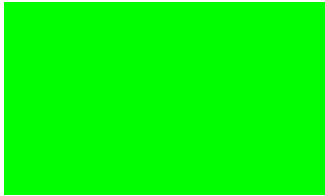



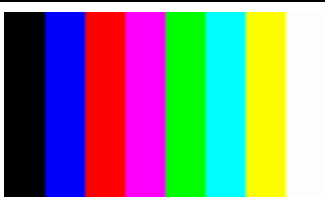
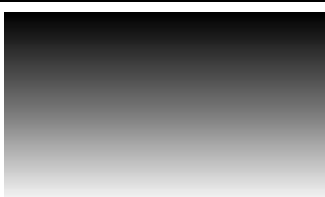
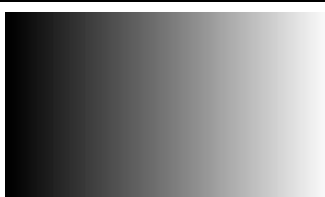
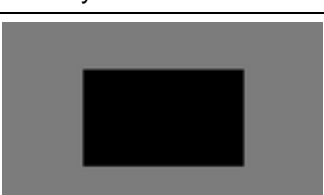
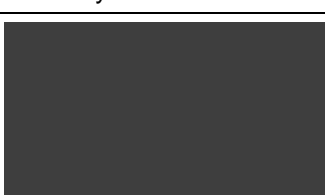
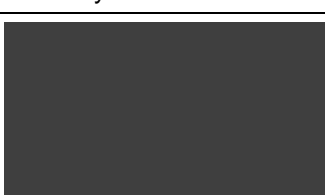
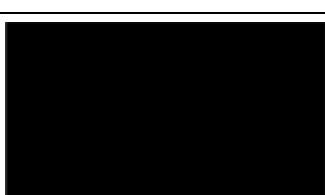
### 5.8. Standby ON/OFF Control

ILI6137A supports Standby mode for saving power consumption, the source driver will turn off and all source output channel will be Hi-Z state when chip in Standby mode. The Standby mode can be controlled via STBYB pin and the Standby ON/OFF timing sequence is illustrated as below:



**5.9. The BIST Patterns for Aging Mode Test**

ILI6137A supports the function to generate BIST patterns for Aging mode test automatically. When external BIST pin goes “H” level, then ILI6137A will leave Normal operation mode and starts to generate the BIST patterns to LCD panel without external clock signal, The BIST patterns is illustrated as below:

1	2	3	4
Red	Green	Blue	Black
			
5	6	7	8
White	Vertical 8-color stripe	Horizontal 64-gray scale	Vertical 64-gray scale
			
9	10	11	12
Gray with black block	Gray with black dot	Gray with black line	Black with white frame
			

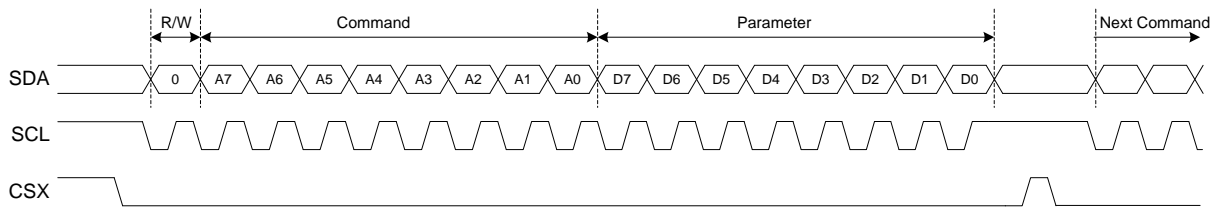
### 5.10. The Command Format for 3-line Serial Interface

ILI6137A using the 3-line serial port as communication interface for all the commands and parameters of CABC function. This 3-line serial communication can be bi-directional controlled by the “R/W” bit in address field. Under read mode, the 3-line engine in ILI6137A will return the data during “Data phase”. The returned data should be latched at the rising edge of SPCK by external controller. Data in the “Hi-Z phase” will be ignored by 3-line engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SPDA pin under “Hi-Z phase” and “Data phase”.

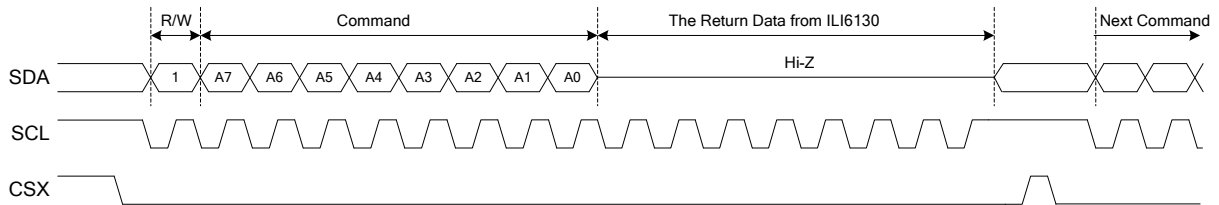
Each Read/Write operation should be exactly 17 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 17 bit data during a CSX Low period will be ignored by 3-line engine.

The timing diagram of read/write operation is illustrated as below:

#### Write Operation



#### Read Operation



## 6. DC Characteristic

### 6.1. Absolute Maximum Rating (VSS = VSSA=0V, Ta=25°C)

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
Power supply voltage 1	VDD	-0.5	--	+5.0	V
Power supply voltage 2	VDDA	-0.5	--	+13.5	V
Gamma correction voltage	V1 ~ V14	-0.5	--	+13.5	V
Input voltage	Vin	-0.3	--	VDD+0.3	V
Operation temperature	TOPR	-20	--	+85	°C
Storage temperature	TSTG	-55	--	+125	°C

Note: (1) All of the voltages listed above are with respect to VSS=VSSA=0V.

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

### 6.2. DC Electrical Characteristics (VSS=VSSA=0V, Ta=25°C)

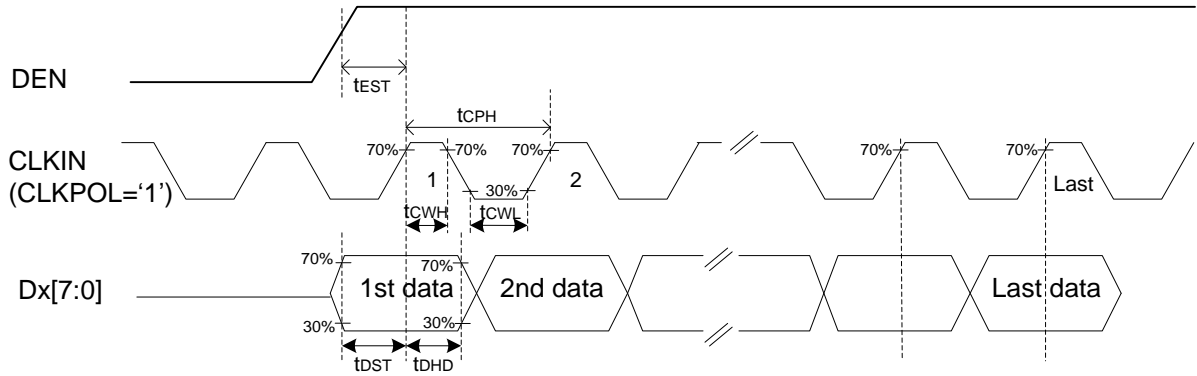
Parameter	Symbol	Spec			Unit	Conditions
		Min.	Typ.	Max.		
Power supply voltage	VDD	3.0	3.3	3.6	V	--
Power supply voltage	VDDA	8.5	10.4	13.5	V	--
Low level input voltage	V <sub>IL</sub>	0	--	0.3*VDD	V	For the digital circuit block
High level input voltage	V <sub>IH</sub>	0.7*VDD	--	VDD	V	For the digital circuit block
Output low voltage	V <sub>OL</sub>	--	--	VSS+0.4	V	IOL=+400μA
Output high voltage	V <sub>OH</sub>	VDD-0.4	--	--	V	IOH=-400μA
Input leakage current	I <sub>IN</sub>	--	--	±1	μA	No pull up or pull down.
Input level of V1~V7	V <sub>REF1</sub>	0.5*VDDA	--	VDDA-0.1	V	Gamma correction voltage input
Input level of V8~V14	V <sub>REF2</sub>	0.1	--	0.5*VDDA	V	Gamma correction voltage input
Output voltage deviation	V <sub>OD1</sub>	--	±20	±35	mV	VO=VSSA+0.1V ~ VSSA+0.5V and VO=VDDA-0.1V ~ VDDA-0.5V
Output voltage deviation	V <sub>OD2</sub>	--	±15	±20	mV	VO= VSSA+0.5V ~ VDDA-0.5V
DC offset	V <sub>OS</sub>	--	--	±20	mV	VO= VSSA+0.5V ~ VDDA-0.5V
Dynamic output range	V <sub>DR</sub>	0.1	--	VDDA-0.1	V	S1 ~ S1200
Pull high/low resistance	R <sub>H</sub>	200	250	300	kΩ	For digital input pins at VDD=3.3V
Output sinking current	I <sub>OL</sub>	80	--	--	μA	S1~S1200, VO =0.1V vs. 1.0V, VDDA=13.5V
Output driving current	I <sub>OH</sub>	80	--	--	μA	S1~S1200, VO=13.4V vs. 12.5V, VDDA=13.5V
Analog operating current	I <sub>DDA</sub>	--	10	12	mA	Without loading, FCLK=50MHz, FLD=48kHz, VDDA=10V, V1=8V, V14=0.4V
Digital operating current	I <sub>DD</sub>	--	8	10	mA	FCLK=50MHz, FLD=48kHz, VDD=3.3V
Analog standby current	I <sub>STBA</sub>	--	10	50	μA	No loading, clock and all functions are stopped
Digital standby current	I <sub>STBD</sub>	--	10	50	μA	Clock and all functions are stopped

Note: VDD=3.0 ~ 3.6V, VDDA=8.5~13.5V, VSS=VSSA=0V, Ta= -20 ~ +85°C

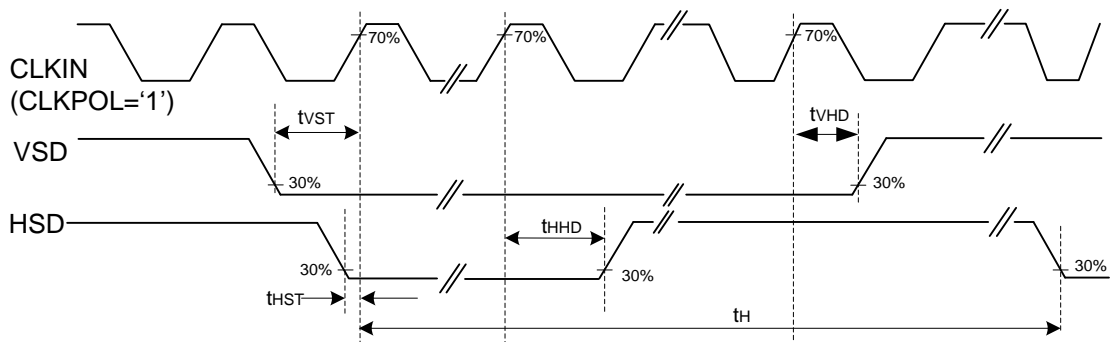
## 7. AC Characteristics

### 7.1. AC Timing characteristics

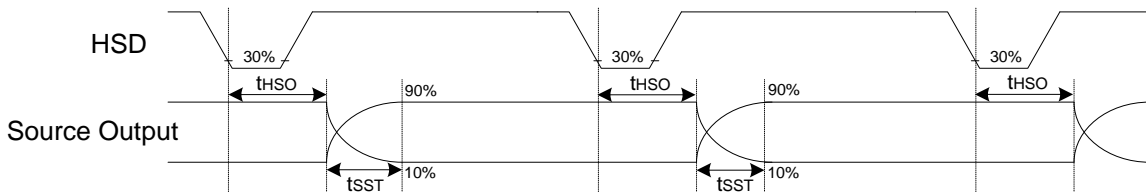
#### DE Mode (MODE= H)



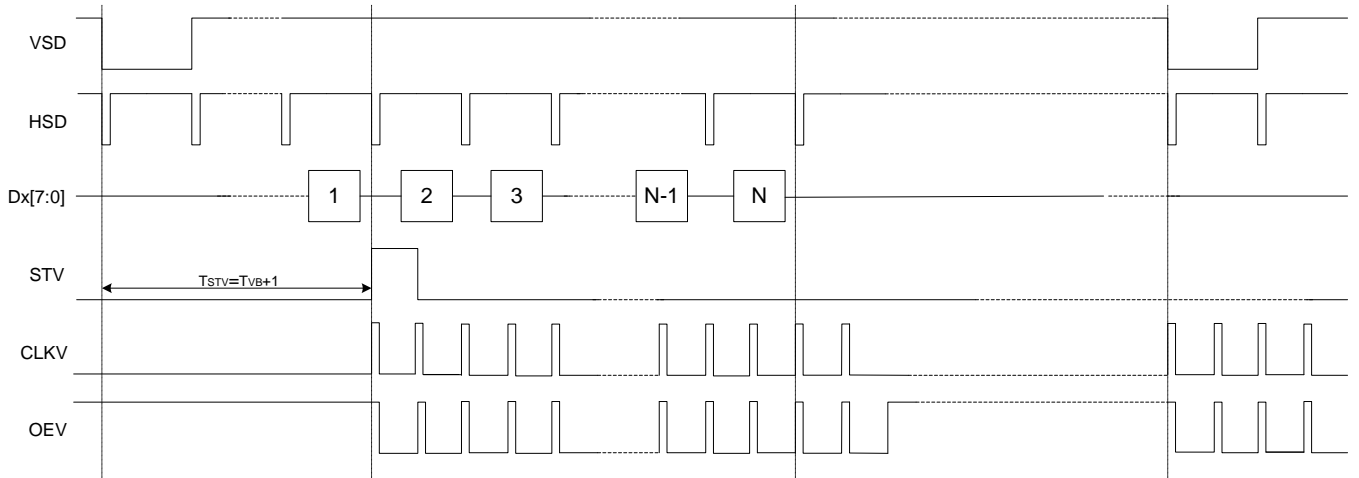
#### SYNC Mode (MODE= L)



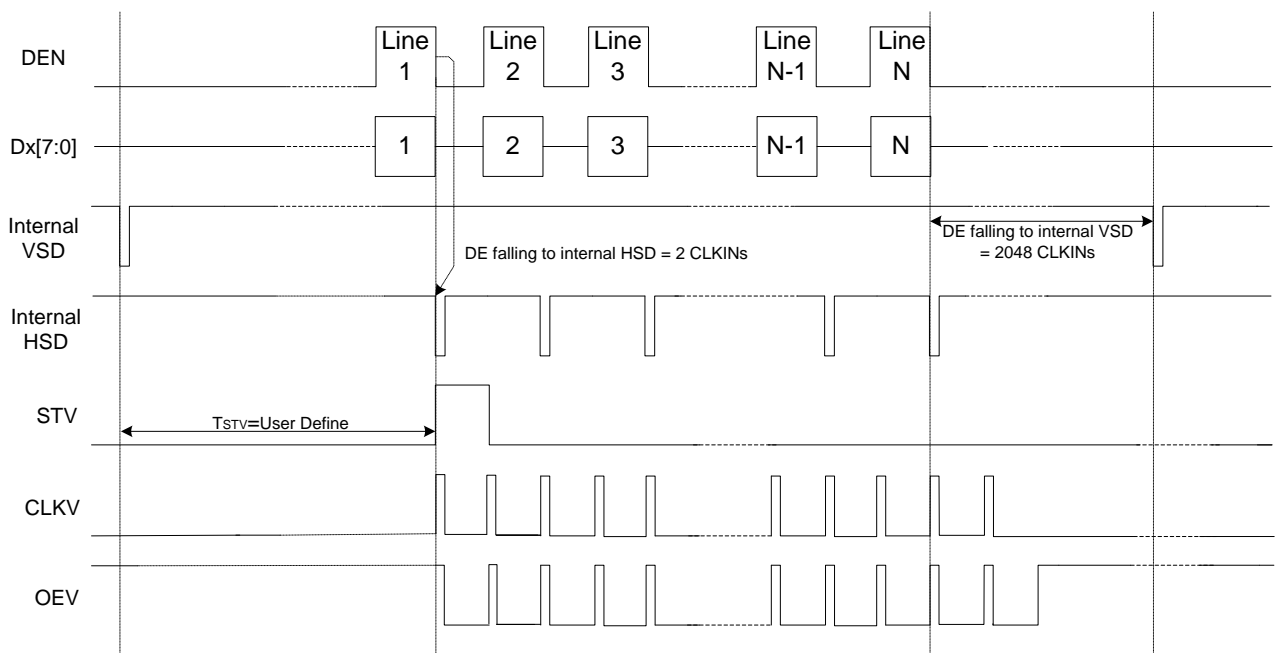
#### Source Output timing Diagram (Cascade)



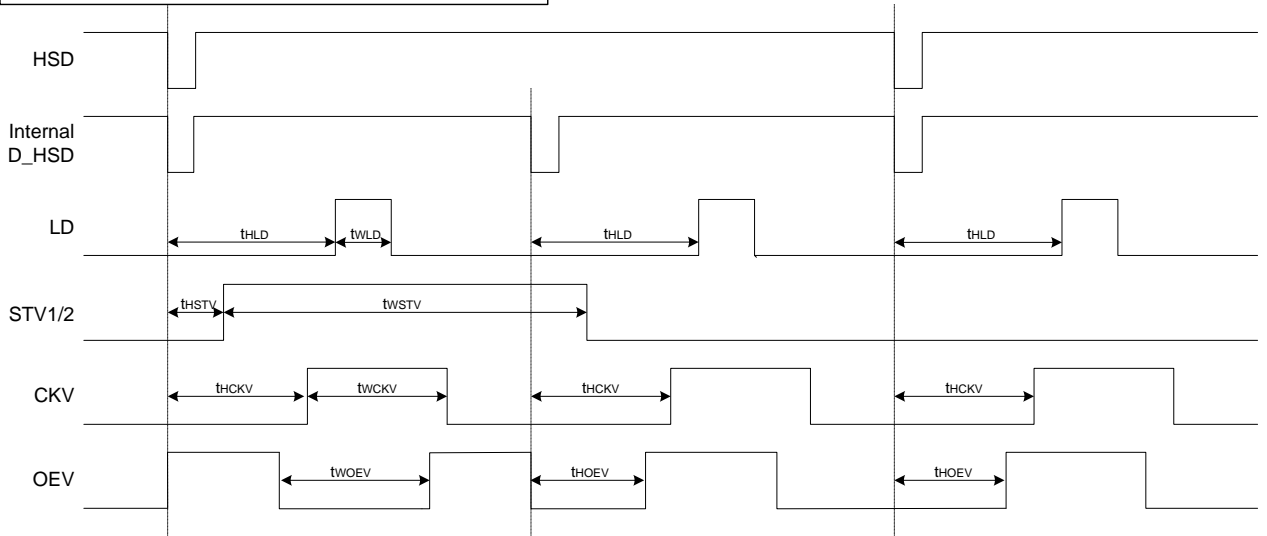
**Vertical Timing Diagram of SYNC Mode (Dual Gate)**



**Vertical Timing Diagram of DE Mode (Dual Gate)**



**Gate Output Timing Diagram (Dual Gate)**

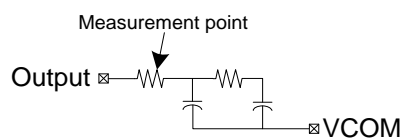


Parameter	Symbol	Spec			Unit	Conditions
		Min.	Typ.	Max.		
VDD Power ON slew rate	t <sub>POR</sub>	--	--	20	ms	0V ~ 0.9*VDD
RSTB pulse width	t <sub>RST</sub>	10	--	--	us	CLKIN=50MHz
CLKIN cycle time	t <sub>CPH</sub>	20	--	--	ns	
CLKIN pulse duty	t <sub>CWH</sub>	40	50	60	%	
VSD setup time	t <sub>VST</sub>	8	--	--	ns	
VSD hold time	t <sub>VHD</sub>	8	--	--	ns	
HSD setup time	t <sub>HST</sub>	8	--	--	ns	
HSD hold time	t <sub>HHD</sub>	8	--	--	ns	
Data setup time	t <sub>DST</sub>	8	--	--	ns	D0[7:0], D1[7:0], D2[7:0] to CLKIN
Data hold time	t <sub>DHD</sub>	8	--	--	ns	D0[7:0], D1[7:0], D2[7:0] to CLKIN
DE setup time	t <sub>EST</sub>	8	--	--	ns	
DE hold time	t <sub>EHD</sub>	8	--	--	ns	
Output stable time	t <sub>SST</sub>	--	--	6	us	10% to 90% target voltage. CL=120pF, R=10KΩ
CLKIN frequency	f <sub>CLK</sub>	--	40	50	MHz	VDD=3.0 ~ 3.6V
CLKIN cycle time	t <sub>CLK</sub>	20	25	--	ns	
CLKIN pulse duty	t <sub>CWH</sub>	40	50	60	%	T <sub>CLK</sub>
Time from HSD to Source output	t <sub>HSD</sub>	--	20	--	CLKIN	
Time from HSD to LD	t <sub>HLD</sub>	--	20	--	CLKIN	Note (2)
Time from HSD to STV	t <sub>HSTV</sub>	--	2	--	CLKIN	
Time from HSD to CKV	t <sub>HCKV</sub>	--	20	--	CLKIN	
LD pulse width	t <sub>WLD</sub>	--	10	--	CLKIN	Note (2)
CKV pulse width	t <sub>WCKV</sub>	--	66	--	CLKIN	
OEV pulse width	t <sub>WOEV</sub>	--	74	--	CLKIN	

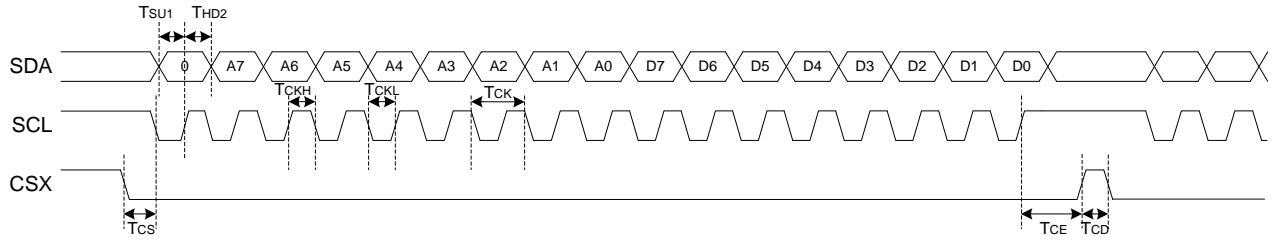
Note: (1) VDD=3.0 ~ 3.6V, VDDA=8.5~13.5V, VSS=VSSA=0V, Ta= -20 ~ +85 °C

(2) The contents of the data register are transferred to the latch circuit at the rising edge of LD. Then the gray scale voltage is output from the device at the falling edge of LD.

(3) Output loading condition:



**SPI Timing**

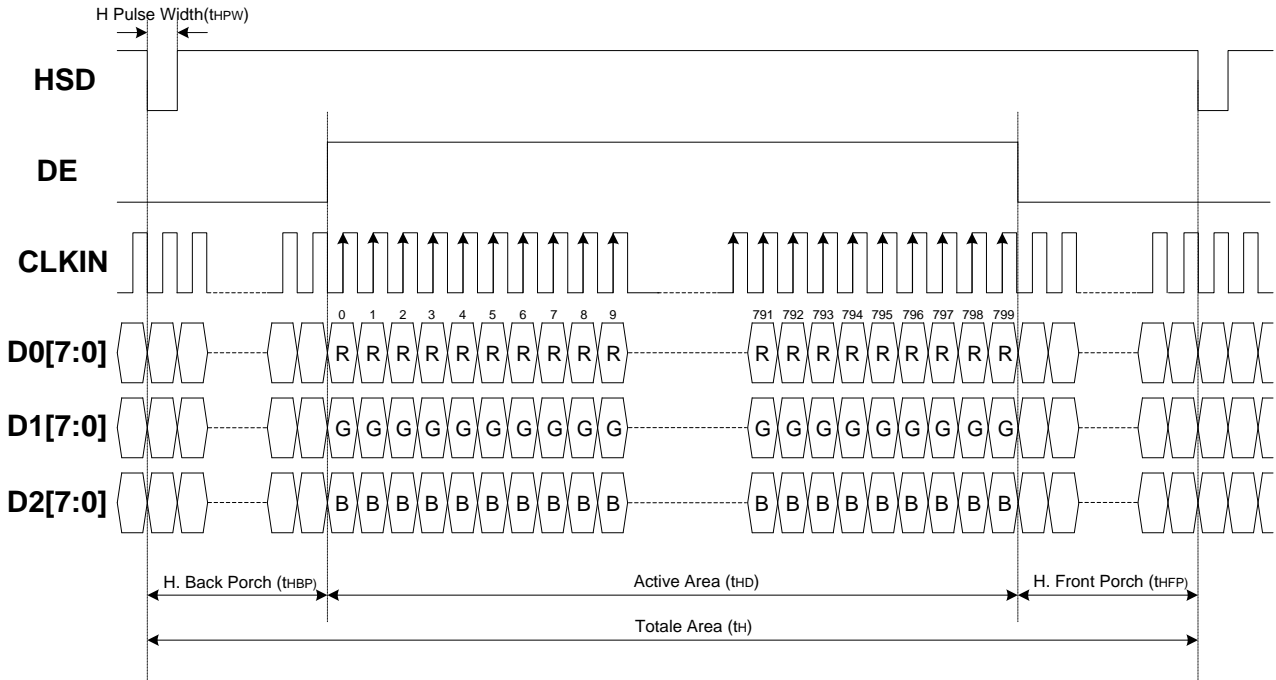


Parameter	Symbol	Spec			Unit	Conditions
		Min.	Typ.	Max.		
SCL period	$T_{CK}$	60	--	--	ns	
SCL high width	$T_{CKH}$	30	--	--	ns	
SCL low width	$T_{CKL}$	30	--	--	ns	
Data setup time	$T_{SU1}$	12	--	--	ns	
Data hold time	$T_{HD1}$	12	--	--	ns	
CSX to SCL setup time	$T_{CS}$	20	--	--	ns	
CSX to SDA hold time	$T_{CE}$	20	--	--	ns	
CSX high pulse width	$T_{CD}$	50	--	--	ns	

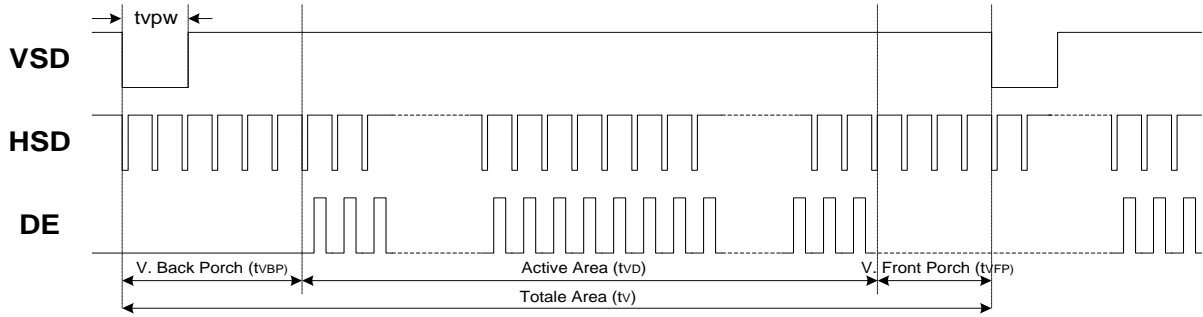


## 7.2. Display Timing characteristics

### 7.2.1. Resolution: 800x480

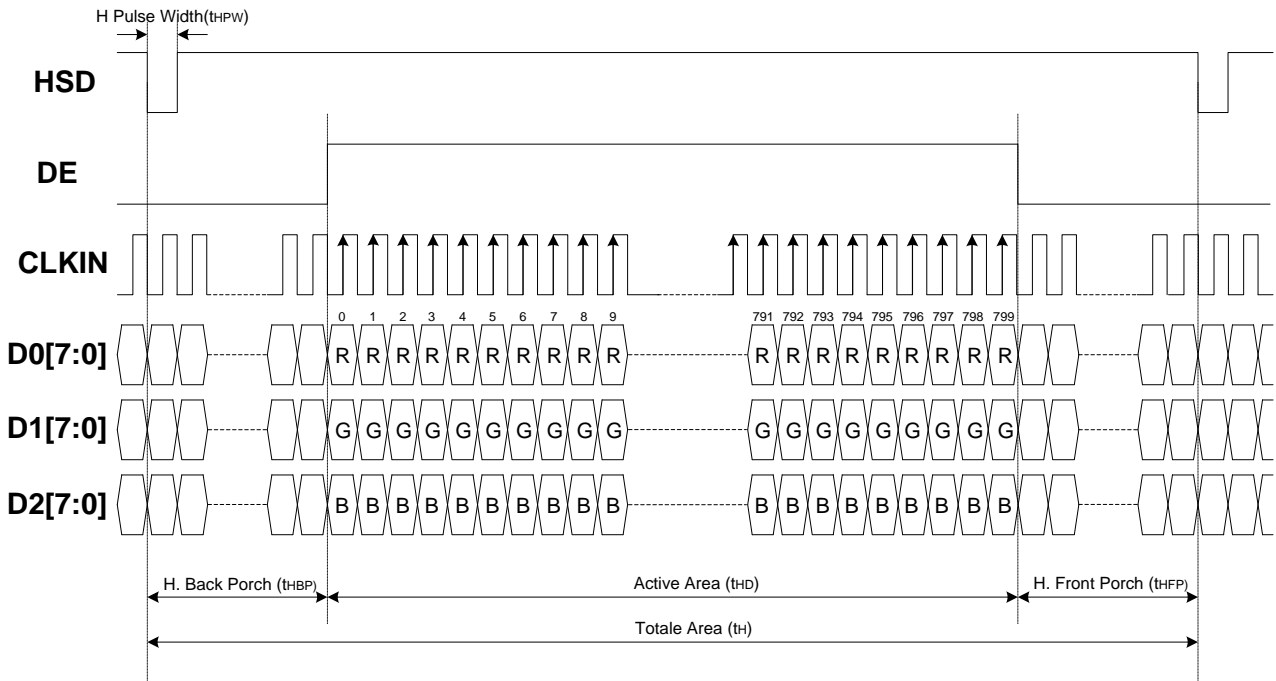


Horizontal Input Timing						
Parameter	Symbol	Value			Unit	
		Min.	Typ.	Max.		
Horizontal display area	t <sub>HD</sub>	--	800	--	CLKIN	
CLKIN frequency	f <sub>CLK</sub>	--	33.3	50	MHz	
1 Horizontal line period	t <sub>H</sub>	862	1056	1200	CLKIN	
HSD pulse width	Min.	--	1	--	CLKIN	
	Typ.	--	--	--	CLKIN	
	Max.	--	40	--	CLKIN	
HSD back porch	SYNC t <sub>HBP</sub>	46	46	46	CLKIN	
HSD front porch	SYNC t <sub>HFP</sub>	16	210	354	CLKIN	

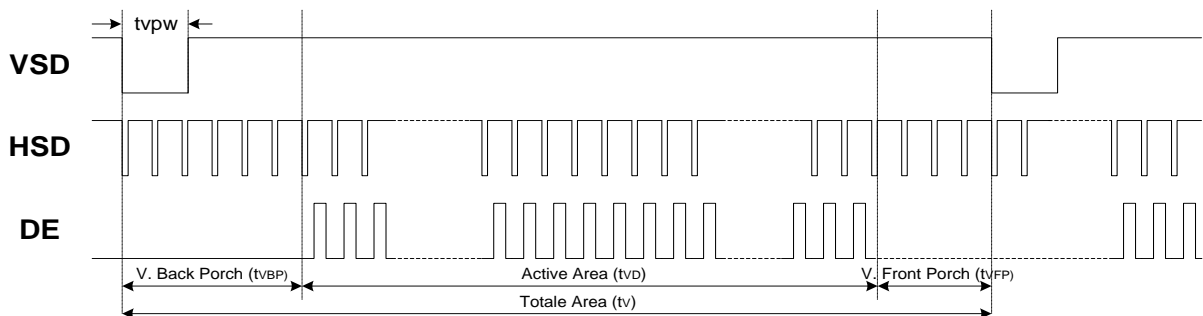


Vertical Input Timing					
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	$t_{vD}$	--	480	--	HSD
VSD period time	$t_v$	510	525	650	HSD
VSD pulse width	$t_{vPW}$	1	--	20	HSD
VSD back porch	$t_{vBP}$	23	23	23	HSD
VSD front porch	$t_{vFP}$	7	22	147	HSD

**7.2.2. Resolution: 800x600**

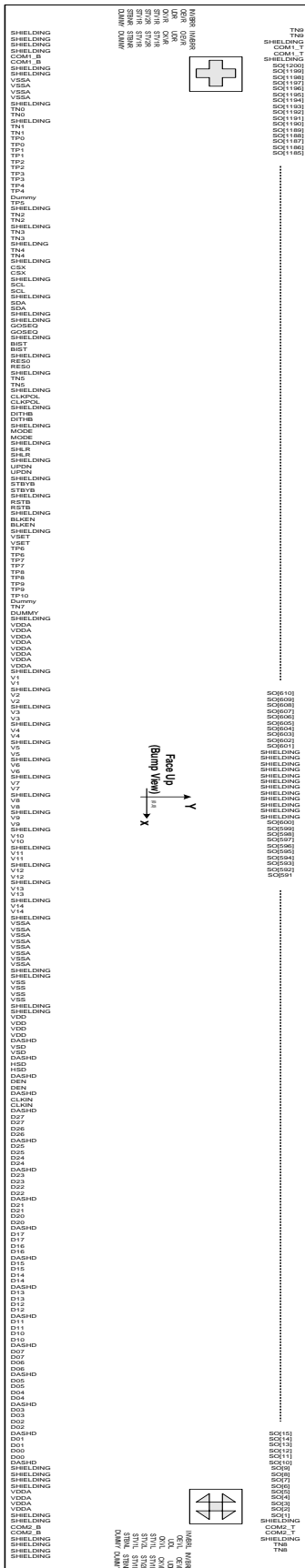


Horizontal Input Timing						
Parameter	Symbol	Value			Unit	
		Min.	Typ.	Max.		
Horizontal display area	$t_{HD}$	--	800	--	CLKIN	
CLKIN frequency	$f_{CLK}$	--	40	50	MHz	
1 Horizontal line period	$t_H$	862	1056	1200	CLKIN	
HSD pulse width	Min.	--	1	--	CLKIN	
	Typ.	--	--	--	CLKIN	
	Max.	--	40	--	CLKIN	
HSD back porch	SYNC	$t_{HBP}$	46	46	46	CLKIN
HSD front porch	SYNC	$t_{HFP}$	16	210	354	CLKIN

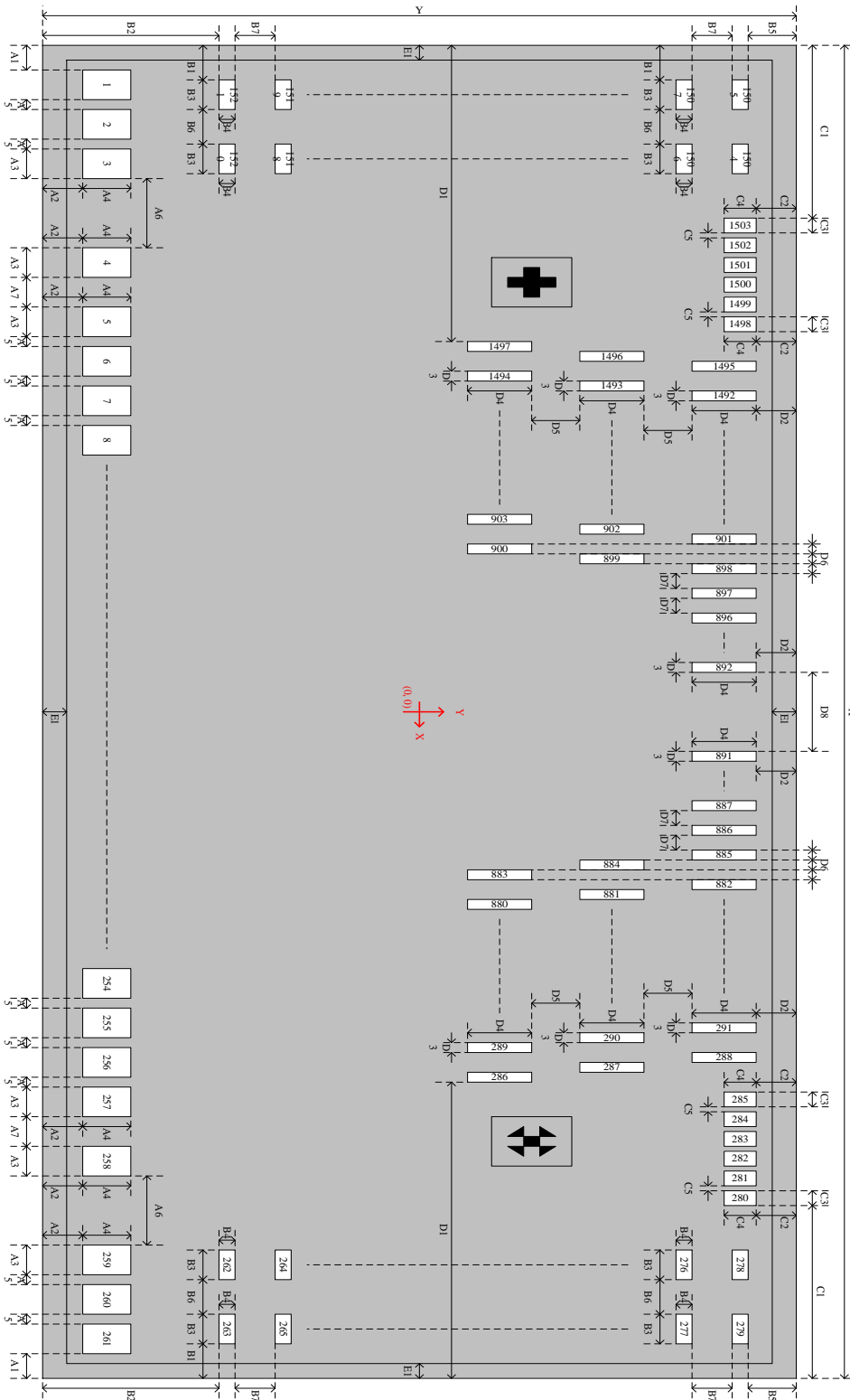


Vertical Input Timing						
Parameter	Symbol	Value			Unit	
		Min.	Typ.	Max.		
Vertical display area	$t_{VD}$	--	600	--	HSD	
VSD period time	$t_V$	624	635	700	HSD	
VSD pulse width	$t_{VPW}$	1	--	20	HSD	
VSD back proch	$t_{VBP}$	23	23	23	HSD	
VSD front porch	$t_{VFP}$	1	12	77	HSD	

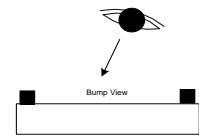
# 8. Pad Sequence (Bump Side)



## 9. Pad Arrangement and Coordination



Symbol	Dimension (um)
A1	48.5
A2	48.5
A3	60
A4	65
A5	25
A6	141.5
A7	55
B1	66
B2	219.5
B3	60
B4	30
B5	58.5
B6	70
B7	50
C1	346
C2	48.5
C3	30
C4	40
C5	20
D1	646
D2	48.5
D3	17
D4	80
D5	60
D6	17
D7	17
D8	450
E1	30
X	22550
Y	948



**Chip size: 22550 um x 948 um(Include 60um scribe line).**

**Chip height: 400 um .**

**Bump height: 9 um .**















No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1393	SO[1096]	-8852.5	385.5	1451	SO[1154]	-9838.5	245.5	1509	UDR	-11179	240.5
1394	SO[1097]	-8869.5	245.5	1452	SO[1155]	-9855.5	105.5	1510	CKVR	-11049	160.5
1395	SO[1098]	-8886.5	105.5	1453	SO[1156]	-9872.5	385.5	1511	CKVR	-11179	160.5
1396	SO[1099]	-8903.5	385.5	1454	SO[1157]	-9889.5	245.5	1512	STV1R	-11049	80.5
1397	SO[1100]	-8920.5	245.5	1455	SO[1158]	-9906.5	105.5	1513	STV1R	-11179	80.5
1398	SO[1101]	-8937.5	105.5	1456	SO[1159]	-9923.5	385.5	1514	STV2R	-11049	0.5
1399	SO[1102]	-8954.5	385.5	1457	SO[1160]	-9940.5	245.5	1515	STV2R	-11179	0.5
1400	SO[1103]	-8971.5	245.5	1458	SO[1161]	-9957.5	105.5	1516	STV1R	-11049	-79.5
1401	SO[1104]	-8988.5	105.5	1459	SO[1162]	-9974.5	385.5	1517	STV1R	-11179	-79.5
1402	SO[1105]	-9005.5	385.5	1460	SO[1163]	-9991.5	245.5	1518	STBNR	-11049	-159.5
1403	SO[1106]	-9022.5	245.5	1461	SO[1164]	-10008.5	105.5	1519	STBNR	-11179	-159.5
1404	SO[1107]	-9039.5	105.5	1462	SO[1165]	-10025.5	385.5	1520	DUMMY	-11049	-239.5
1405	SO[1108]	-9056.5	385.5	1463	SO[1166]	-10042.5	245.5	1521	DUMMY	-11179	-239.5
1406	SO[1109]	-9073.5	245.5	1464	SO[1167]	-10059.5	105.5				
1407	SO[1110]	-9090.5	105.5	1465	SO[1168]	-10076.5	385.5				
1408	SO[1111]	-9107.5	385.5	1466	SO[1169]	-10093.5	245.5				
1409	SO[1112]	-9124.5	245.5	1467	SO[1170]	-10110.5	105.5				
1410	SO[1113]	-9141.5	105.5	1468	SO[1171]	-10127.5	385.5				
1411	SO[1114]	-9158.5	385.5	1469	SO[1172]	-10144.5	245.5				
1412	SO[1115]	-9175.5	245.5	1470	SO[1173]	-10161.5	105.5				
1413	SO[1116]	-9192.5	105.5	1471	SO[1174]	-10178.5	385.5				
1414	SO[1117]	-9209.5	385.5	1472	SO[1175]	-10195.5	245.5				
1415	SO[1118]	-9226.5	245.5	1473	SO[1176]	-10212.5	105.5				
1416	SO[1119]	-9243.5	105.5	1474	SO[1177]	-10229.5	385.5				
1417	SO[1120]	-9260.5	385.5	1475	SO[1178]	-10246.5	245.5				
1418	SO[1121]	-9277.5	245.5	1476	SO[1179]	-10263.5	105.5				
1419	SO[1122]	-9294.5	105.5	1477	SO[1180]	-10280.5	385.5				
1420	SO[1123]	-9311.5	385.5	1478	SO[1181]	-10297.5	245.5				
1421	SO[1124]	-9328.5	245.5	1479	SO[1182]	-10314.5	105.5				
1422	SO[1125]	-9345.5	105.5	1480	SO[1183]	-10331.5	385.5				
1423	SO[1126]	-9362.5	385.5	1481	SO[1184]	-10348.5	245.5				
1424	SO[1127]	-9379.5	245.5	1482	SO[1185]	-10365.5	105.5				
1425	SO[1128]	-9396.5	105.5	1483	SO[1186]	-10382.5	385.5				
1426	SO[1129]	-9413.5	385.5	1484	SO[1187]	-10399.5	245.5				
1427	SO[1130]	-9430.5	245.5	1485	SO[1188]	-10416.5	105.5				
1428	SO[1131]	-9447.5	105.5	1486	SO[1189]	-10433.5	385.5				
1429	SO[1132]	-9464.5	385.5	1487	SO[1190]	-10450.5	245.5				
1430	SO[1133]	-9481.5	245.5	1488	SO[1191]	-10467.5	105.5				
1431	SO[1134]	-9498.5	105.5	1489	SO[1192]	-10484.5	385.5				
1432	SO[1135]	-9515.5	385.5	1490	SO[1193]	-10501.5	245.5				
1433	SO[1136]	-9532.5	245.5	1491	SO[1194]	-10518.5	105.5				
1434	SO[1137]	-9549.5	105.5	1492	SO[1195]	-10535.5	385.5				
1435	SO[1138]	-9566.5	385.5	1493	SO[1196]	-10552.5	245.5				
1436	SO[1139]	-9583.5	245.5	1494	SO[1197]	-10569.5	105.5				
1437	SO[1140]	-9600.5	105.5	1495	SO[1198]	-10586.5	385.5				
1438	SO[1141]	-9617.5	385.5	1496	SO[1199]	-10603.5	245.5				
1439	SO[1142]	-9634.5	245.5	1497	SO[1200]	-10620.5	105.5				
1440	SO[1143]	-9651.5	105.5	1498	SHIELDING	-10664	405.5				
1441	SO[1144]	-9668.5	385.5	1499	COM1_T	-10714	405.5				
1442	SO[1145]	-9685.5	245.5	1500	COM1_T	-10764	405.5				
1443	SO[1146]	-9702.5	105.5	1501	SHIELDING	-10814	405.5				
1444	SO[1147]	-9719.5	385.5	1502	TN9	-10864	405.5				
1445	SO[1148]	-9736.5	245.5	1503	TN9	-10914	405.5				
1446	SO[1149]	-9753.5	105.5	1504	INVBRR	-11049	400.5				
1447	SO[1150]	-9770.5	385.5	1505	INVBRR	-11179	400.5				
1448	SO[1151]	-9787.5	245.5	1506	OEVR	-11049	320.5				
1449	SO[1152]	-9804.5	105.5	1507	OEVR	-11179	320.5				
1450	SO[1153]	-9821.5	385.5	1508	UDR	-11049	240.5				

## 10. Revision History

Version No.	Date	Page	Description
0.01	2019/04/18	All	New set up
0.02	2022/04/21	11	Added TP5 Defination